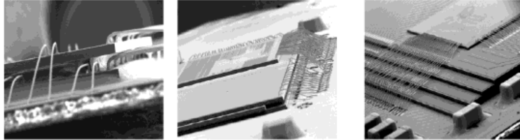
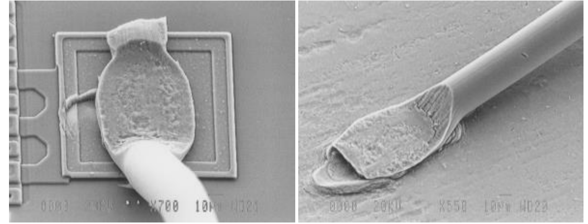
Micro and Nano- Electronics Reliability
Classical approach and new trends



Part 3 - Packaging and assemby reliability
Metallisations

Chip-Package connection

- Wire bond techniques
- Tape Automatic bonding
- Flip-Chip



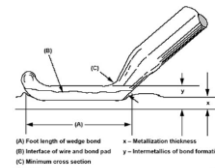
Analysis performed by Bernard PLANO - IMS

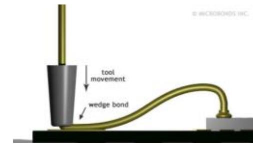
Wire-bonding

- Connections are made from the chip to the pad frame via thin wires
  - Typically 100x100 µm metal pads on 200 µm pitch
  - Mechanical bonding of one pin at a time (sequential)
- The Wires materials : low resistivity alloys or doped metals
  - Gold and Aluminum
  - Copper and Silver
- Typically 25 µm diameter for logic devices

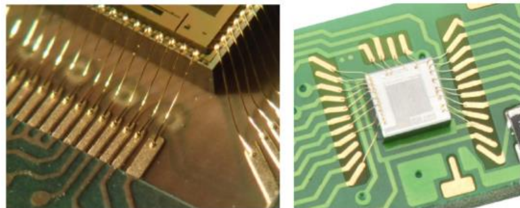
https://www.youtube.com/watch?v=th1YxQHEpEU

Wedge Bonding



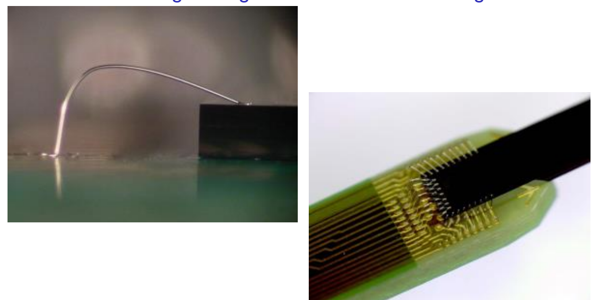


Gold wire-bonding



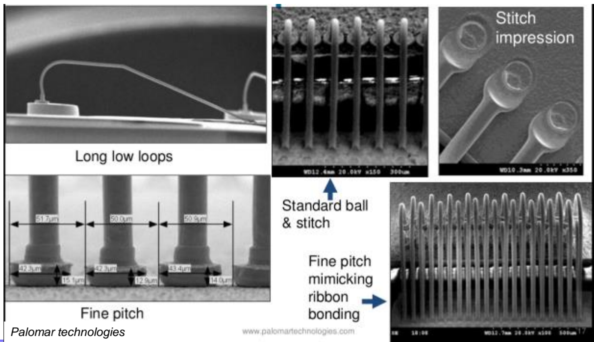
http://www.buf-bonding.de

Wedge-wedge Aluminium wire-bonding



http://www.buf-bonding.de

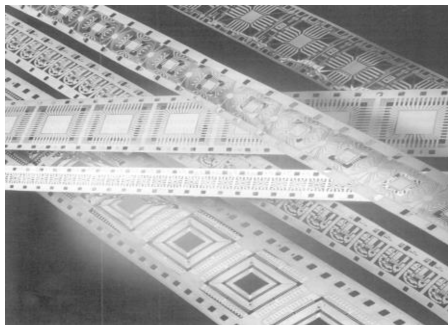
Other examples



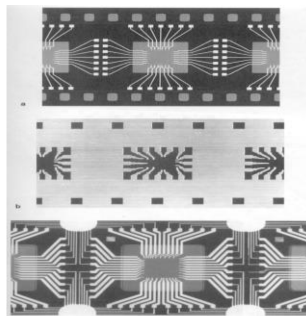
Wire-bonding : drawbacks

- Slow process
  - One pin at a time ; 4 to 10 wires per second
- Pads limited to the chip periphery
  - Low pad density and reduced pad pitch
  - Up to approximately 500 pads
- Electrical limitations
  - High inductance (~1nH) of wires (~10nH plus pins)
  - Crosstalk between adjacent wires

Chip To Package Interconnection : Tape Automated Bonding



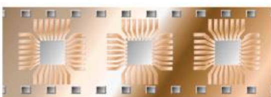
Chip To Package Interconnection : Tape Automated Bonding

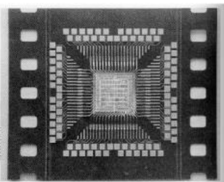


- Tape-automated bonding (TAB) is a process that places bare integrated circuits onto a flexible printed circuit board (FPC) by attaching them to fine conductors in a polyamide or polyimide film, thus providing a means to directly connect to external circuits
- TAB was created as an alternative to wire bonding and finds common use by manufacturers in LCD display driver circuits.[3]

https://www.youtube.com/watch?v=X104jJNTvuc

TAB





- Interconnections patterned on a multilayer polymer tape.
- Tape positioned above the `bare die' so that the metal tracks (on the polymer tape) correspond to the bonding sites on the die
- Advantages over wire bonding
  - Smaller and closer pads
    - higher density, up to 850 pins
    - Better electrical characteristics
  - Faster procedure but more expensive machinery

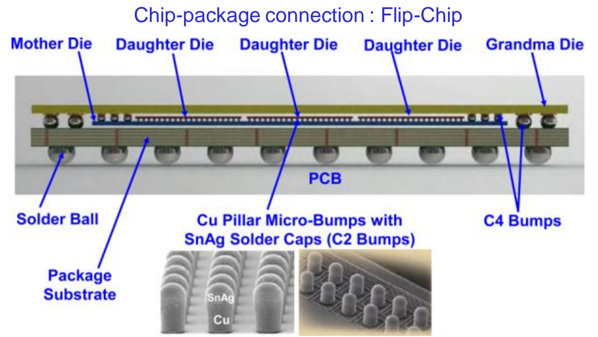
Chip-package connection : Flip-Chip

- The chip is “soldered” to the package substrate using the solder balls “bumps” that have been grown over the die pads
- Flip-chip is currently the preferred process for high-end integrated circuits
- High frequency of operation, small size and/or many I/O pins

Chip-package connection : Flip-Chip

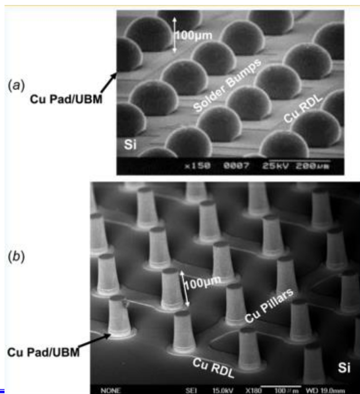
- Advantages
  - ➢ Improved density: pad pitch and size is not better than in wire bonding, but I/O pads can be distributed all over the die, not just in the borders
  - ➢ Reduced inductance (~0.1 nH) due to the elimination of wires and better power/ground behavior
  - ➢ Faster process, all the pads are soldered at the same time
- Some drawbacks
  - ➢ Alignment is critical (and blind), although there is some tolerance due to its self-alignment property
  - ➢ Mechanical stress due to different thermal expansion coefficients of the silicon and the package substrate

Chip-package connection : Flip-Chip



3D IC packaging (Amkor's multiple chip-to-chip interconnects)

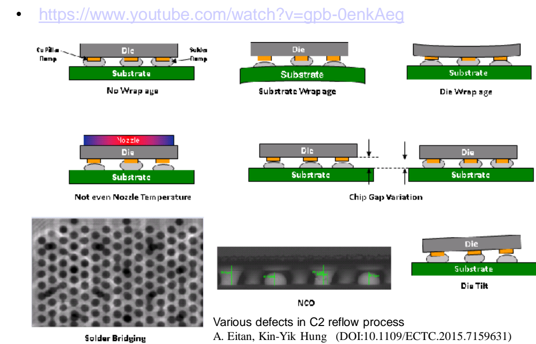
- Lau JH. Recent Advances and New Trends in Flip Chip Technology. ASME. J. Electron. Packag. 2016;138(3):030802-030802-23. i:10.1115/1.4034037



- Lau JH. Recent Advances and New Trends in Flip Chip Technology. ASME. J. Electron. Packag. 2016;138(3):030802-030802-23. i:10.1115/1.4034037

Copper pillar

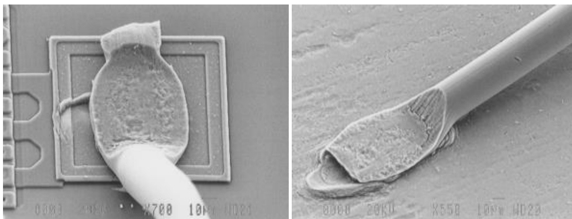
- https://www.youtube.com/watch?v=gpb-0enkAeg



Various defects in C2 reflow process
A. Eitan, Kin-Yik Hung (DOI:10.1109/ECTC.2015.7159631)

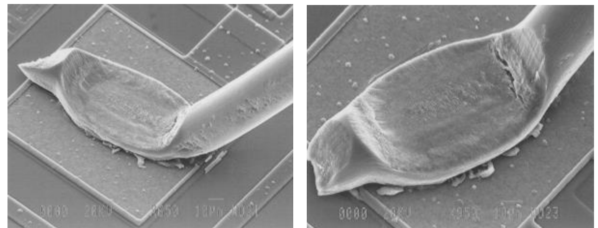
Chip-Package connection reliability: focus on wire bond

Failure modes
Failure mechanisms
Case studies



Analysis performed by Bernard PLANO - IMS

Chip to package interconnection : wire bonding



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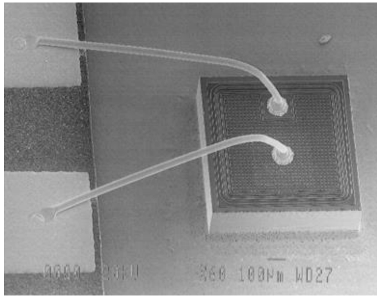

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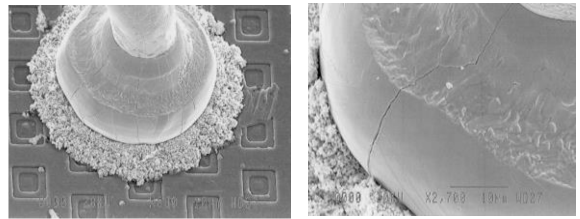
Chip to package interconnection : wire bonding



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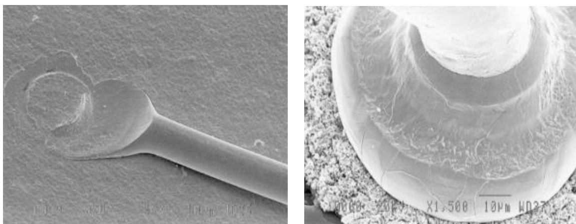
Chip to package interconnection : wire bonding



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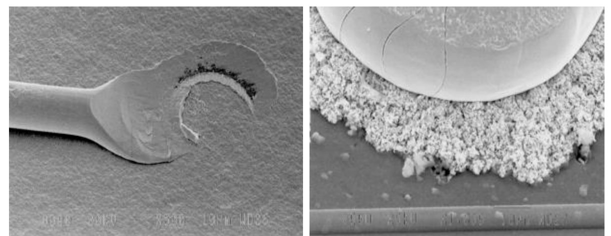
Chip to package interconnection : wire bonding



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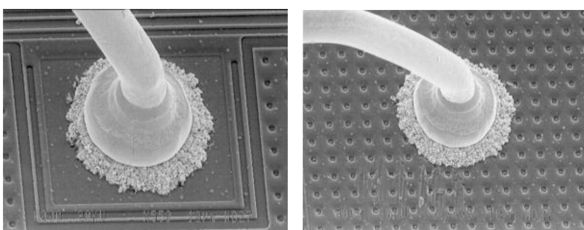
Chip to package interconnection: wire bonding



Analysis performed by Bernard PLANO - IMS

Wire bond failure modes

Wire bond has to make electrical connection
R increases up to open circuits

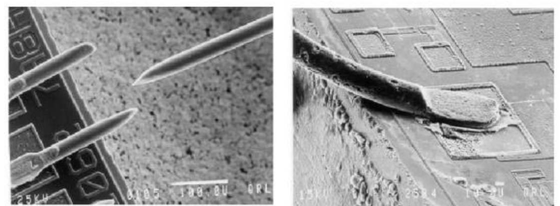


Figure 1. One mil diameter aluminum wired after tensile overstress.

Figure 2. Corrosion has dissolved aluminum from bond pad and wire causing open circuit.

Case Studies of Metallurgical Failure Mechanisms in Microelectronics –R. Haythornthwaite Chipworks Inc

Wire bond failure mechanisms

Causes	Mechanisms
Temperature	Intermetallic compounds growth
Moisture	Corrosion
Contaminants	Break of the wire
Thermal-mechanical effects	

Intermetallic compounds

• IMC is a class of substances composed of definite proportions of two or more elemental metals

• Intermetallic compounds are often simply called 'alloys', although this is a poor description

• Intermetallic compounds are generally brittle and have a high melting point.
• The Intermetallic Compounds formation occurs between solder and metallization pad

http://nepp.nasa.gov/wirebond/intermetallic_creation_and_growt.htm

Intermetallic Creation and Growth

• Intermetallic compounds form when two unlike metals diffuse into one another.

• Diffusion is enabled by the movement of atoms of one material into the crystal vacancies of the other material (crystal vacancies made available by defects, contamination, impurities, grain boundaries and mechanical stress).

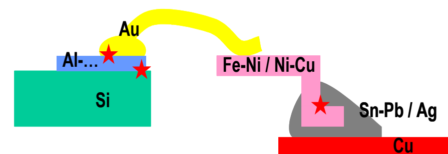
• The diffusion rates are a function of temperature.

• Diffusion and void creation during the formation of intermetallic materials was studied by Kirkendall and so the voids created have often been called Kirkendall voids.

http://nepp.nasa.gov/wirebond/intermetallic_creation_and_growt.htm

Intermetallic Growth

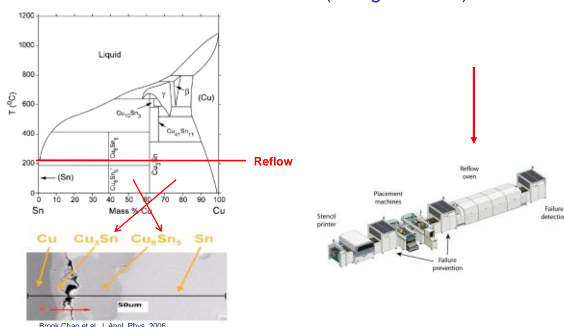
Different metals in contact



"Slow" diffusive phenomena (Fick's law)
→ formation of new compounds (T_{fusion} ↓)
→ modification of properties at the interfaces

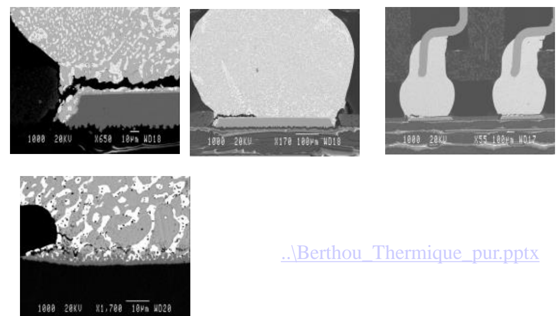
- Electrical (resistivity)
- Mechanical (Young's modulus, resilience)
- Geometric (eg : Kirkendall effect)

IMC- Kinetics of Growth (SnAgCu -SAC)



Brook Chao et al. J. Appl. Phys. 2006

Intermetallic in solder balls: examples



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Intermetallic Creation and Growth
Au/Al wire bonds

• For the Au/Al bonding case, there are five different intermetallic compounds that can form.

• These intermetallic compounds are always present in Au/Al bonds and should not be associated with the cause of weak bonds.

• Their appearance and location can often be indicators of the conditions and results of the bonding event (incomplete bonds and contaminated bond materials for example).

• Excessive Kirkendall voiding can result in out-of-tolerance wire bond resistance and weakened wire bonds.

http://nepp.nasa.gov/wirebond/intermetallic_creation_and_growt.htm

Intermetallic Creation and Growth
Au/Al wire bonds

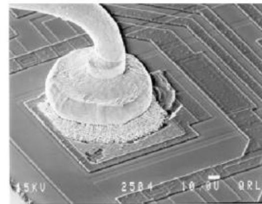
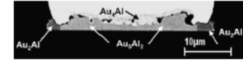
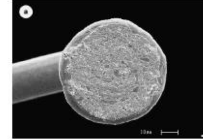


Figure 4. Formation of gold aluminum intermetallics between the gold wire and the square aluminum bond pad. Note the depletion of aluminum surrounding the intermetallics.



SEM, BE image of an Au ball bond on Al–1%Si–0.5%Cu bondpad after 200 h ageing in air at 175 C.

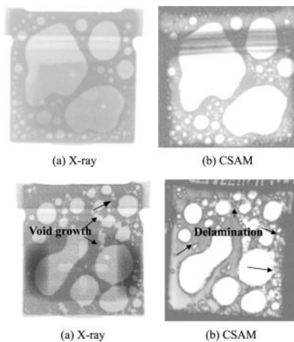


SEM, SE image of the underside of a typical gold ball after removal from a bondpad. Light areas are regions of intermetallic.

Case Studies of Metallurgical Failure Mechanisms in Microelectronics –R. Haythornthwaite Chipworks Inc

C.D. Breach, F. Wul. / Microelectronics Reliability 44 (2004) 973–981

kirkendall Effect



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