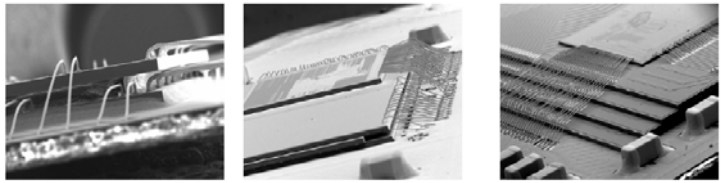
Micro and Nano- Electronics Reliability
Classical approach and new trends

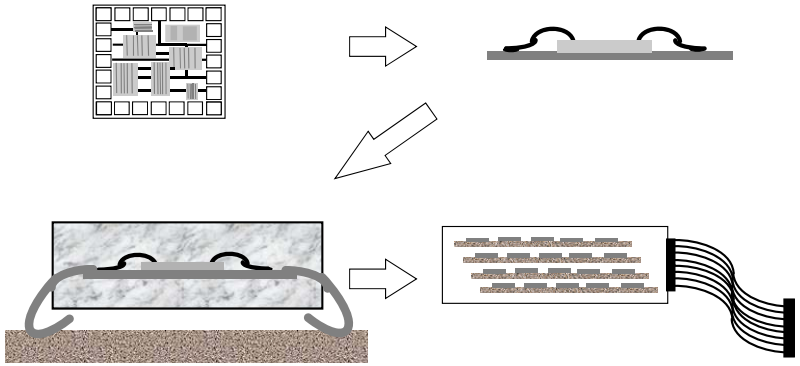
Part 3 - Packaging and assembly reliability



Layout

- Introduction
- Technological considerations
- Degradation mechanisms (focus on Pem)
  - General mechanisms
  - New mechanisms
- Reliability evaluation
  - Tests
  - "Physics of Failure" approach
- Conclusion

Definitions



Packaging functions

Signal Distribution

→ Topologic and electromagnetic considerations

Power Distribution

→ Structural, material and electromagnetic considerations

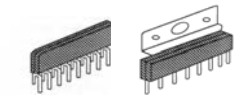
Thermal Dissipation

→ Structural, and material considerations

Protection

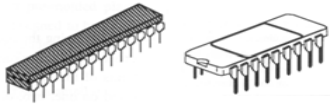
→ Mechanical, chemical and electromagnetic of components and interconnections

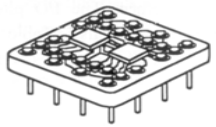
Mounting technologies and case types
Pin through hole mounting



SIP and ZIP : « Single et Zigzag In line Package »
Leads only on 1 side on the case

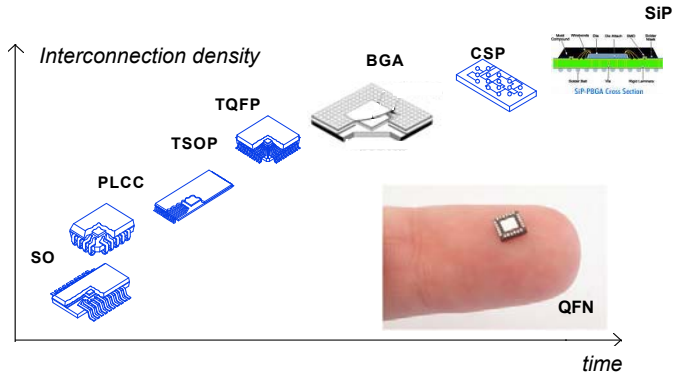
DIP : « Dual in line package »
Leads on both sides





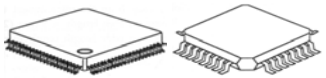
• PGA : « Pin Grid Array »
leads distributed above the case

Case evolution



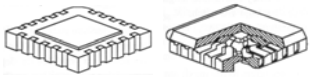
Mounting technologies and case types
SMD Surface Mounted Devices

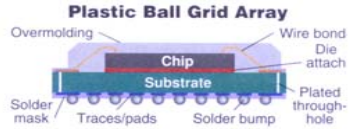
SOP : Small Outline Package



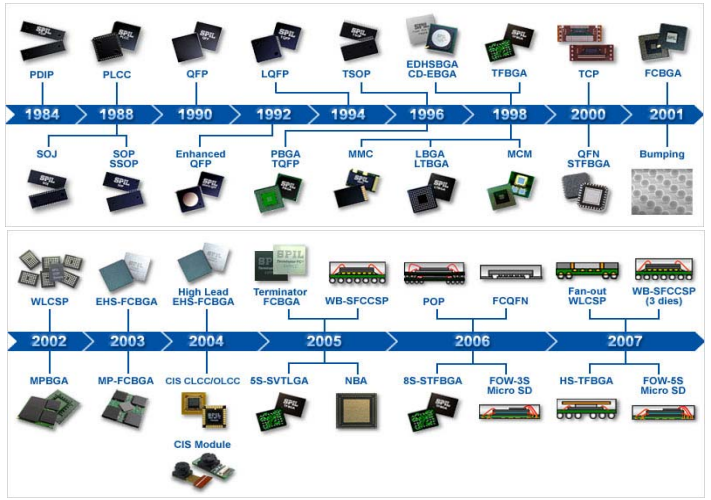
QFP : Quad FlatPack

CC : Chip carrier





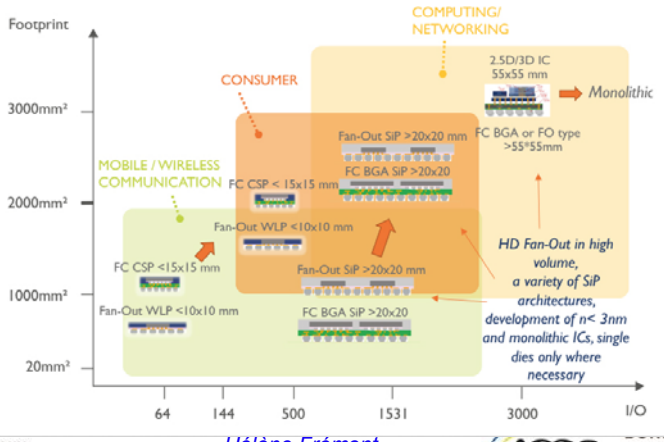
BGA : Ball Grid Array



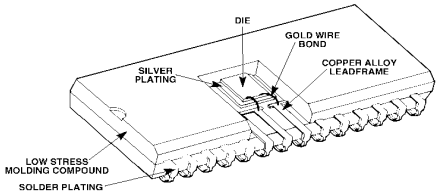
Siliconware Precision Industries Co http://www.spil.com.tw

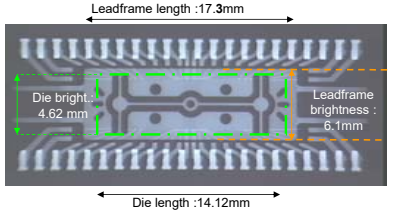
Flip-chip and fan-out packaging - vision for 2030

(Source: Status of the Advanced Packaging Industry 2018, Yole Développement, September 2018)



Example of a small leaded package : SOJ 44

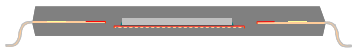




Diversity in plastic encapsulation: examples

SOJ 36 Samsung

TQFP 160 Cypress



SBGA 352 Xilinx

HQFP 240 Xilinx

In a similar package: increasing density and complexity

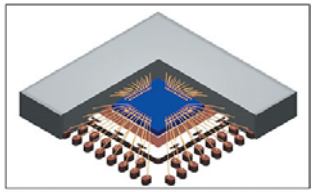


Figure 1: ELP packages can be configured with multiple rows of lead frame pads and power/ground ring options.

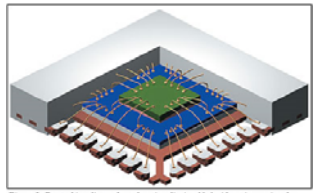


Figure 2: By stacking die, package functionality is added without increasing the package footprint.

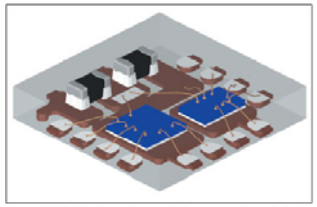


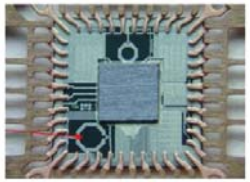
Figure 3: SiP technology is emerging as a reliable and lower-cost alternative to substrate based MCMs and SOC designs.

https://www.ecnasiamag.com/article-9739-leadframesleadtheway-Asia.html

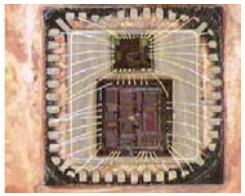
Advanced Interconnect Technologies

SiP

"System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system."

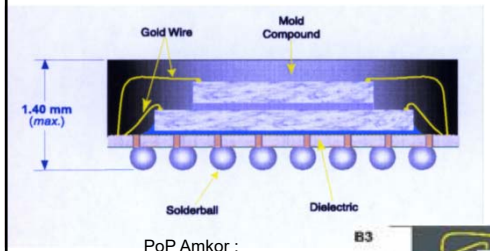


NXP



Freescale

Examples

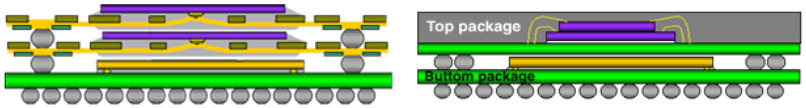


Stacked CSP Amkor : 2 stacked dies

PoP Amkor : 2 stacked packages

Akita electronics Japan

PoP Stack Up



Examples

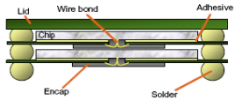
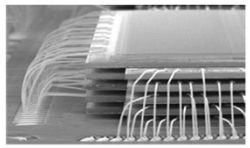
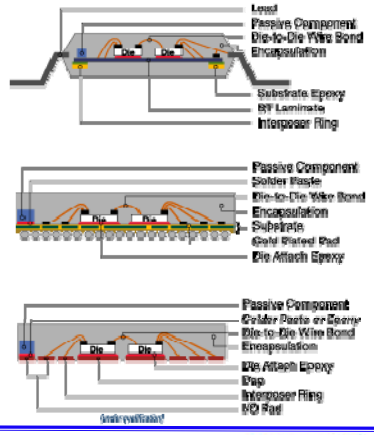


Fig. 2. Schematic view of a Multi-stack Package (MSP)

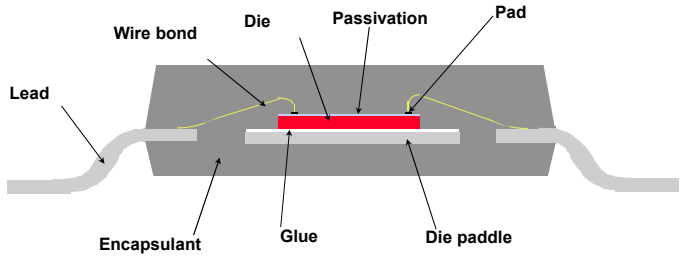
S.Y. Yang et al. / Microelectronics Reliability 46 (2006) 1904–1909



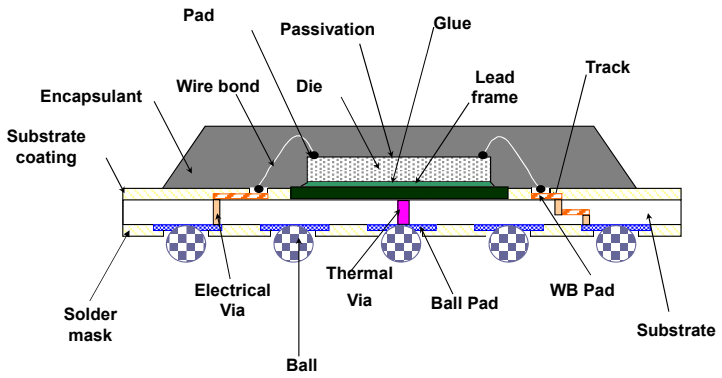
Asat.com



Technologic model of a leaded package



Technologic model of a BGA

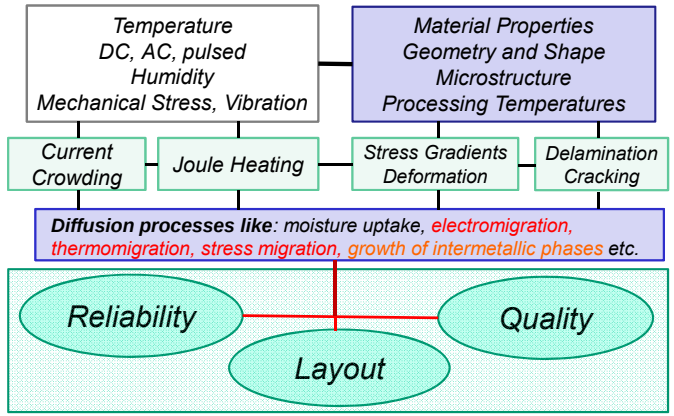


General degradation mechanisms

- Temperature
- Thermal cycling
- Humidity
- Contamination
- Solid Particles
- Pressure
- Vibrations
- Mechanical cycling
- Radiations
- Heavy particles

→ (Inter)diffusions
→ Oxidation
→ Chemical reactions
→ Photolyse
→ Corrosion
→ Mechanical fatigue
→ Cracking
→ Crack propagation
→ Delamination
→ Abrasion
→ EOS
→ Cristal degradation
→ Charge trapping

Failure mechanisms in packages and assemblies

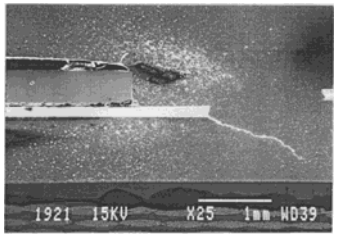


Plastic packages issues

Stresses in Plastic encapsulated devices

Sources
- Encapsulation
- Soldering on substrate
- Thermal cycling and gradients
- Moisture Absorption

Associated Failures
- Deformation of metallizations
- Corrosion
- Interfacial delamination
- Depolymerization of plastic
- Cracks in the plastic



Prevention
- Prediction by modelling and simulation
- ATC (assembly test chip) measurements

Failure mechanisms linked to plastic package

Corrosion (Chemical or electro-chemical degradation of metallization)

Cause : contaminants
Influent factors : temperature, humidity, electrical field
Test methods : hot moisture with or without bias

Tests at 85°C/85%RH
THB (temperature humidity bias) idem + inverse biasing
HAST (high accelerated stress test), 100 to 175°C ; RH 50 to 85%.

Corrosion (Chemical)

•Physico-chemical transformation of materials with "loss" of (useful) material
- – Intrinsic: functional materials
- –"Semi-intrinsic" : residue from manufacturing processes
- –Extrinsic: contribution and influence of environmental species
  - •purple plague + Kirkendall catalyzed by H_2O and halogens
  - •galvanic corrosion in the presence of water
  - •redox
  - •oxidation
  - •other chemical reactions (eg salt media)

•Main victims: metallizations
- –On-Chip Interconnect
- –Intra-case
- –External Connections: assembly and interconnection

•Locations :
- –Surface (oxidation)
- –Where protection is defficient
- –At interfaces

Kinetics and impact vary widely depending on:
Materials | Medium
Protections

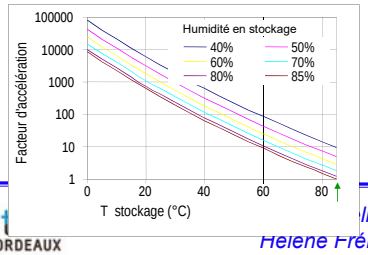
Oxidation in moist atmosphere

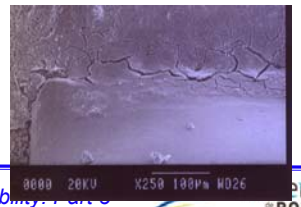
Eyring's law

$$t_{corr} = A(RH)^{n} e^{\frac{E_a}{kT}}$$

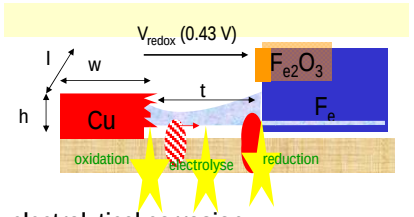
$E_a \approx 0.9$ eV (usual materials)
$n \approx -3$ (empirical)
depends on:
- materials
- geometry
- criterion

Remarks : - is empirically used for life times
- false for RH<20% or RH → 100%





Galvanic corrosion



Water + pollutant : S, SO_2, SO_3

redox couples :
Fe^{3+}/Fe^{2+} (0.77V)
Cu^{2+}/Cu (0.34 V)
H_3O^+/H_2O (0.00 V)
...

• electrolytical corrosion

• Complex and multiple phenomena
• Big influence of pollutants (acides, H_2, N_2...)

•Howard model

$$t_{cor} = \frac{w^2\, h\, l\, n_c\, \gamma\, F_f}{m\, V} \frac{\rho_{elec}}{t_{elec}}$$

rem : difficult to apply because of lack of control

Failure mechanisms linked to plastic package

Metallisation deformations

maximum at the IC edges
increase with IC size

Cause : Thermal - mechanical stresses
Influent factor : temperature
Test methods : Thermal cycles

Plastic depolymerization (liquefaction)

Mechanism starting at high temperatures
(190 to 230 °C for epoxies and 260°C for silicones)

Cause : breakage of polymer bonds
Influent factor : temperature
Test methods : temperature re-bake

Failure mechanisms linked to plastic package

Interfacial cracking and delamination

Cause : Thermal - mechanical stresses
Influent factors : temperature and moisture
Test methods : Thermal cycles or shocks with moisture preconditionning

Moisture influence on delamination

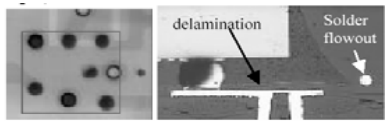


Fig. 1: Typical failure after MSL preconditioning reflow

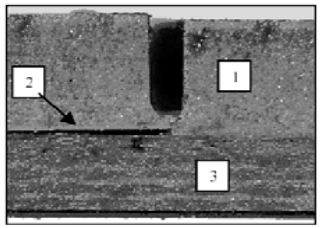
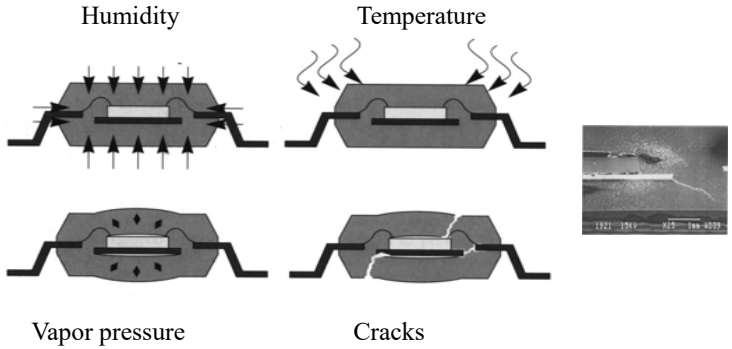


Fig. 5: The observed crack along the substrate-solder resist interface (1 = molding compound, 2 = solder resist, 3 = substrate.)

Coefficient of moisture expansion taken into account

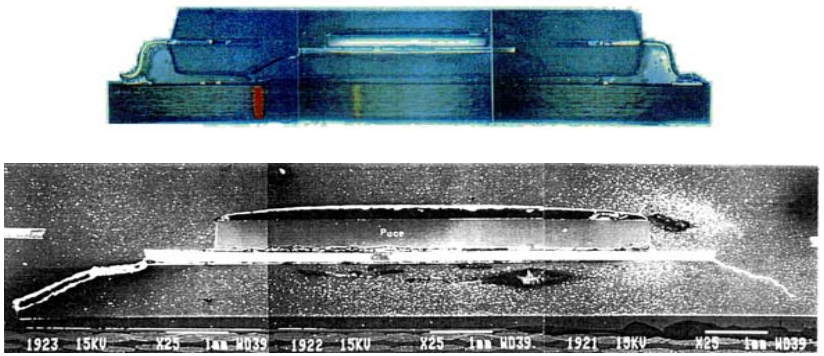
Characterization and Modelling of Moisture Driven Interface Failures M.A.J. van Gils, et al ESREF 2004

Moisture influence on delamination: pop corn effect



Major issue during reflow process

Moisture influence on delamination: pop corn effect

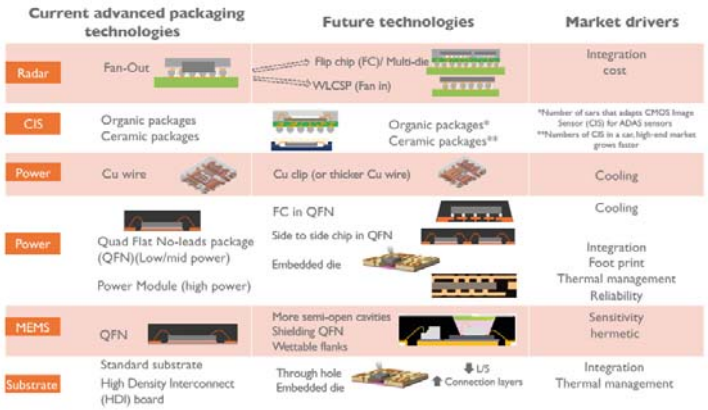


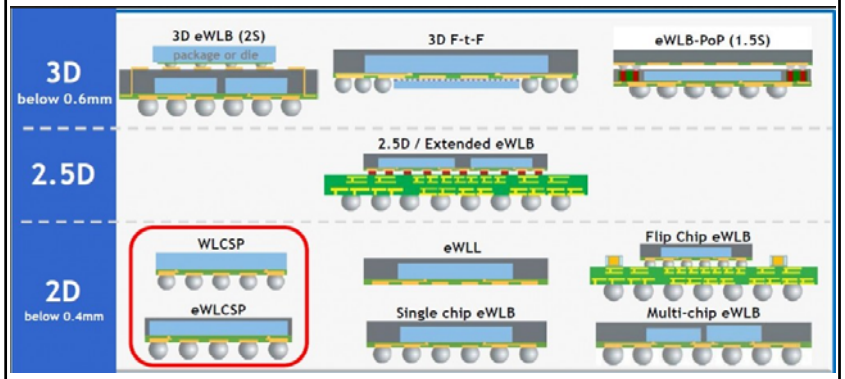
Analysis by Bernard PLANO - IMS

Emerging technologies issues

Automotive packaging roadmap

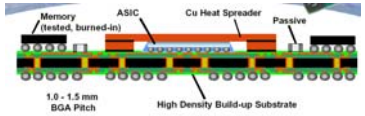
(Source: Trends in Automotive Packaging 2018, Yole Développement, November 2018)





Technology evolution: worsening the stresses

- At Chip level
  - Dimension increase
  - Diversification of functions (SoC)
  - Higher power density
  - Higher frequencies
  - ….



- At package and assembly levels
  - Densification of internal interconnections (SiP)
  - Juxtaposition of RF, analog, digital and power blocks,
  - New material (lead free solders)
  - More aggressive processes (PoP)
  - New dimensions of stresses (3D)

Technology evolutions + Harsh environment : Increasing the risks

- Thermal Effects
  - Thermal Gradients within the chip (SoC)
  - Thermal Gradients within the package (SiP)
  - Close to « Power electronics » problems
- Specific components
  - Passive (capacitive, inductive structures…)
  - Specific Quality/Reliability requirements
- Mechanical stresses
  - Third dimension
  - Multiple and miscellaneous interfaces
- EMC

Qualification / reliability tests still adapted ?

Technological variations

Applications for New Materials

- In this decade most if not all packaging materials will change due to changing functional and regulatory requirements
  - Bonding wire
  - Molding compounds
  - Underfill
  - Thermal interface materials
  - Die attach materials
  - Substrates
  - Solder

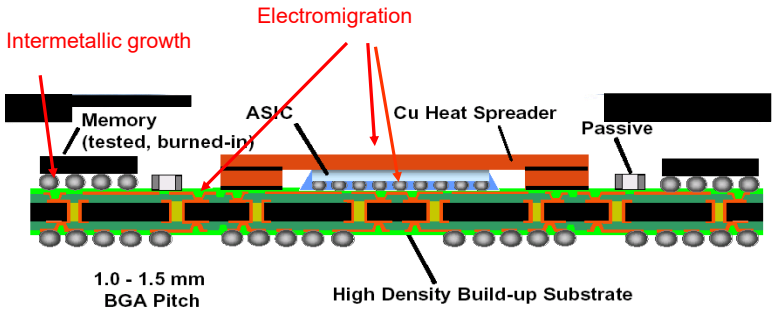
ITRS Winter Conference 2007 Kamakura, Japan 11

- Rapid evolution
- Less process control

Probable critical mechanisms

- Electromigration
  - Interconnection (Cu) on chip (SoC) : high power consumption
  - Vias and interconnections on intermediate PCB (PoP)
  - Lead free bumps in flip-chip
- Intermetallics
  - Lead free
- Thermal-mechanical effects
  - Gradients
  - « 3D Effects »

Probable critical mechanisms



+ Cracks, interfacial delaminations

Some tracks for reliability control of electronic systems

- Selection of relevant technologies
- Design for reliability (IC, Board systems)
- In situ structures for stress detection and measurements
- Development of accurate failure mechanisms models
- Role of FE simulation: multiphysics
- Mixed models
- Reliability active monitoring (for systems)