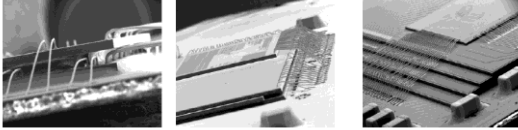


Micro and Nano- Electronics Reliability Classical approach and new trends

Part 1: Introduction



Quality - Reliability and Qualification

- **Quality** : degree of conformance of a product to the applicable specifications, guidelines and workmanship criteria.
- **Reliability** : extend to which a product performs its intended function under stated conditions during a specified period of time
- **Qualification** : includes all activities which ensures that the nominal design and the manufacturing will meet or exceed the reliability targets.

Definitions: failure mode and mechanism

- Failure mechanism
 - The physical, chemical, electrical, thermal or other process that results in failure
- Failure modes, or observable failure events
 - Short-circuits (diodes, transistors, capacitors ...)
 - Open circuits (capacitors, resistors ...)
 - Parametric degradation
 - Limited performance

DEFINITIONS

Failure – Failure rate

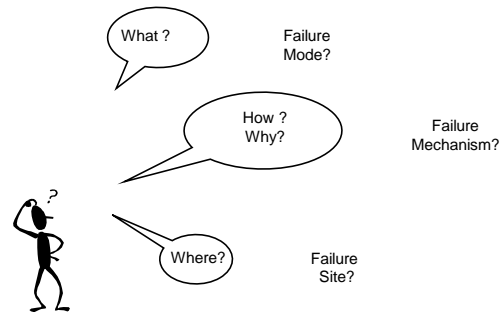
- **Failure** is the inability of the product to perform its defined mission. Failures of electronic devices, in general, can be catastrophic or non-catastrophic.
 - Catastrophic failures render the device totally nonfunctional,
 - Non-catastrophic failures result in an electrically operating device that shows parametric degradation and limited performance.
- The **failure rate** is the frequency with which an engineered system or component fails, expressed in failures per unit of time. The failure rate of a system usually depends on time, with the rate varying over the life cycle of the system (repairable systems)
- The **failure rate** is the total number of failures within an item population, divided by the total time expended by that population, during a particular measurement interval under stated conditions (batch of components)

Failure mechanisms: some examples

- **FEoL Failure Mechanisms**
 - Time-Dependent Dielectric Breakdown (TDDB) – gate oxide
 - Hot Carrier Injection (HCI)
 - Negative Bias Temperature Instability (NBTI)
 - Surface inversion (mobile ions)
 - Floating-Gate Nonvolatile Memory Data Retention
 - Localized Charge Trapping Nonvolatile Memory Data Retention
 - Phase Change (PCM) Nonvolatile Memory Data Retention

Failure mechanisms: some examples

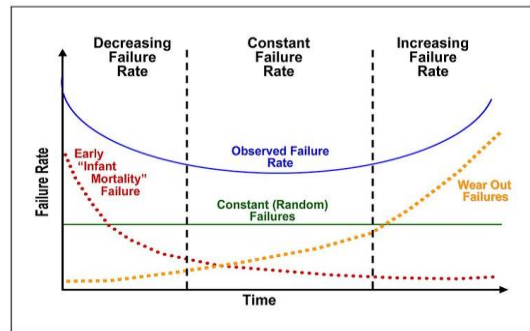
- **BEoL Failure Mechanisms**
 - Time-Dependent Dielectric Breakdown (TDDB)
 - Electromigration
 - Corrosion
 - Stress Migration (AI SM)
- **Packaging/Interfacial Failure Mechanisms**
 - Fatigue failure due to temperature cycling and thermal shock
 - Interfacial failure due to temperature cycling and thermal shock
 - Intermetallic and oxidation failure
 - Tin Whiskers
 - Ionic Mobility Kinetics (PCB) – Component Cleanliness



Classification of failures

- **Intrinsic Failures:** due to the system it-self
 - Material
 - Design
 - Fabrication process
 - Assembly / packaging
- **Extrinsic Failures:** due external loads
 - Electrical Overstress (EOS) / Electrostatic discharges (ESD)
 - Handling / manipulation
 - Specification exceeded (thermal, electrical, chemical, mechanical)
 - Incorrect use

Failure rate as a function of time: "bathtub curve"

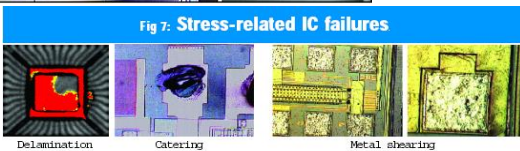


The failure rate of a system usually depends on time, with the rate varying over the life cycle of the system.

Overstress failure: examples



« IC technology and failure mechanisms »
E. Moulin
Industry perspective
June 2004

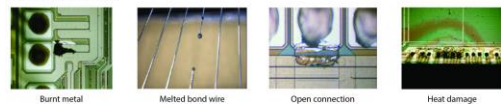


Electrical overstress (EOS) examples

Typical external EOS damage



Typical internal EOS damage



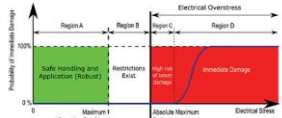
from <http://www.cypress.com/file/97816/download>

Electrical overstress (EOS) and ESD



• EOS	Amount of stress (spec was exceeded)	quantity of stress
• ESD	Kind of stress (discharging of C)	quality of stress

• EOS and ESD are *not alternatives* to each other; ESD can be a *cause* of EOS damage



How absolute maximum ratings should be interpreted. Blue line is the number of components suffering immediate, catastrophic EOS damage.

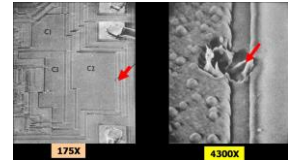
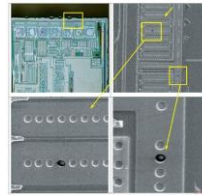
<http://compliancemag.com/articles/interpreting-electrical-overstress/>



Microelectronics Reliability Introduction



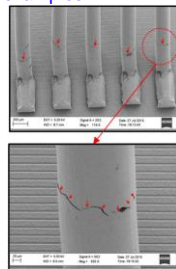
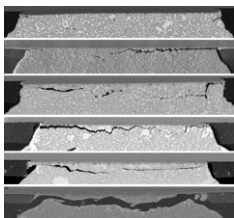
ESD induced failures



Microelectronics Reliability Introduction



Wear-out failures: examples



Improved Physical Understanding of Intermittent Failure in Continuous Monitoring Method
W. Maia, M. Bizoux, H. Frémont, Y. Danto
Microelectronics and Reliability, 2006.

Power cycling test and failure analysis of molded Intelligent Power IGBT Module under different temperature swing durations
U.M. Choi, F. Blaabjerg, S. Je Jørgensen, F. Iannuzzo, H.Wang, C. Uhrenfeldt, S. Munk-Nielsen, Microelectronics Reliability 2016.

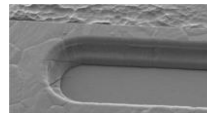


Microelectronics Reliability Introduction



Failure Mechanisms

- Failure mechanisms of electronic semiconductor devices can be divided into the following general categories:
 - (1) Material-interaction-induced mechanisms.
 - (2) Stress-induced mechanisms.
 - (3) Mechanically induced failure mechanisms.
 - (4) Environmentally induced failure mechanisms.



Typical passivation cracks on large Al areas of a typical power IC metallization layer coated with SiN after 1000 T-cycles between -65°C and +175°C.
Ackert, J., et Al. (ICICD7 2015).



Microelectronics Reliability Introduction



Failure Mechanisms

- Material-induced mechanisms can in turn be subdivided into two general categories
 - Semiconductor die material and metal interactions
 - Die packaging and interconnect.
- Stress-induced failure mechanisms can be directly attributed to either poor device design or poor and careless device application.
- Environmentally induced failure mechanisms can cover a wide spectrum of possible environmental conditions
 - Humidity
 - Temperature
 - Chemical agents
 - Mechanical fatigue



Microelectronics Reliability Introduction



Failure Modes and Mechanisms: Example

Table 4-1. Common MMIC failure modes.

Failure Mode	Method of Detection	Related Failure Mechanisms	Possible Solutions
Degradation in I_{DSS}	Life test, operation	Gate sinking, surface effects, hydrogen effects	Derating criteria, temperature control, environmental control
Degradation in gate leakage current	Life test, high-temperature storage test, high-temperature reverse bias	Interdiffusion	Temperature control, gate current control, proper passivation
Degradation in V_p	Life test, operation	Gate sinking, hydrogen effects	Temperature control, use of stable barrier materials, environmental control
Increase in R_{DS}	Life test, operation	Gate sinking, ohmic contact degradation	Temperature control, use of stable barrier materials
Decrease in P_{OUT}	Life test, operation	Surface effects, hydrogen effects, gate sinking	Temperature control, use of stable barrier materials, environmental control



Microelectronics Reliability Introduction



Failure sites, mechanisms and condition monitoring (examples on IGBT)

Failure sites		Failure modes	Failure mechanisms	CM Parameters
Die level	Die	Short circuit, burnout, loss of gate control	Latch-up and secondary break-down	$V_{CE, on}$ t_{off} $V_{GE, th}$
			Time dependent dielectric break-down	V_{GE} $V_{GE, th}$
Package level	Bonding wire: bond	Bond wire liftoff	Fatigue and/or reconstruction	t_{on} t_{off} $V_{CE, on}$ V_{GE}

Failure sites, mechanisms and condition monitoring (examples on IGBT) (2)

Failure sites		Failure modes	Failure mechanisms	CM Parameters	
Package level	Bonding wire: heel	Bond wire heel cracking	Fatigue		
			Open wire	Stress corrosion	
			Wire burnout	Joule heating	
	Solder joint	Solder joint cracks	Fatigue or grain growth	$R_{th, v}$ $V_{CE, on}$ t_{off} Low-order harmonics	

FEOL related failure modes and mechanisms examples in CMOS devices

Failure Mechanisms

- Time Dependent Dielectric Breakdown (TDDB)
- Bias Temperature Instability (BTI)
- Hot Carrier Injection (HCI)
- Mobile Ion Contamination
- Plasma-processing Induced Damage (PPID)
- Random Telegraph Noise (RTN)
- Electrostatic Discharge (ESD)
- Latch-up
- Soft Error Rate (SER), ...

Failure Modes

- Gate current increase
- Threshold voltage shift
- Drain current degradation
- ...

Why learn about Reliability?

Microelectronics reliability in its context

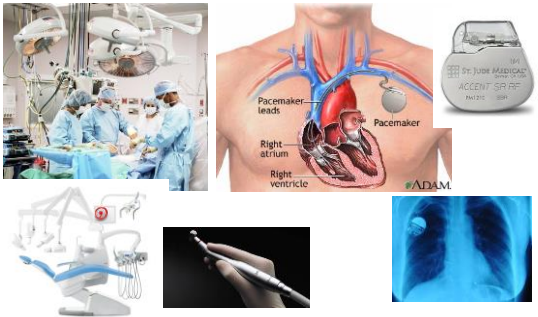
DIVERSIFICATION OF SEMICONDUCTOR PRODUCTS



Microelectronics reliability in its context



Microelectronics reliability in its context



Real Case

- Malfunction identified in pacemaker microprocessor which may lead to single chamber atrial pacing
- Potential of being catastrophic for pacemaker dependent patients with total AV nodal block.
- Number of units distributed: **144000** units
- Failure rate: **0.00014**
- **1371** elective explants resulting from the advisory notice.
- **8** failures identified in the **1371** devices (**0.006%**). One having the potential for serious patient injury.
- **No serious injury reported.**

Microelectronics reliability in its context



Microelectronics reliability in its context

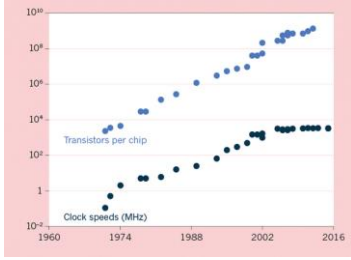


The challenges

The challenges

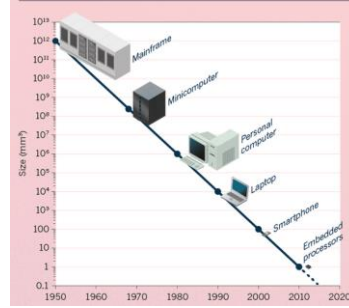
- Moore's Laws
 - Since the invention of the integrated circuit in 1958, the number of transistors that can be placed inexpensively on an integrated circuit has increased exponentially, doubling approximately every two years. The trend was first observed by Intel co-founder Gordon E. Moore in a 1965 paper. It has continued for almost half a century and in 2005 was not expected to stop for another decade at least.
- More than Moore's
- Beyond CMOS: Emergent technologies

Moore's Laws



<https://www.nature.com/news/the-chips-are-down-for-moores-law-1.19338>
 Mitchell Waldrop - Nature 2016 (source Intel)

Moore's Laws

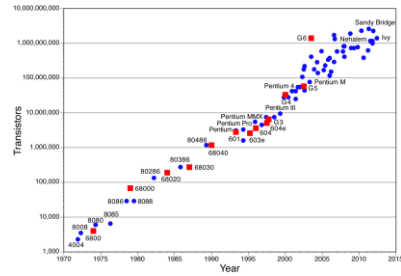


<https://www.nature.com/news/the-chips-are-down-for-moores-law-1.19338>
 Mitchell Waldrop - Nature 2016
 source SIA/SRC

Moore's Laws

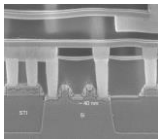
- Almost every measure of the capabilities of digital electronic devices is strongly linked to Moore's law: [processing speed](#), [memory capacity](#), sensors and even the number and size of [pixels](#) in [digital cameras](#).
- All of these are improving at (roughly) [exponential](#) rates as well. This has dramatically increased the usefulness of digital electronics in nearly every segment of the world economy.
- Moore's law describes this driving force of technological and social change in the late 20th and early 21st centuries.

Moore's law for memory chips and microprocessors

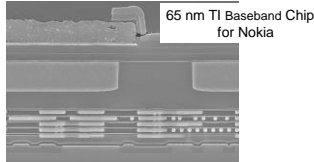


The uppermost purple curve is the Moore projection based on data up to 1975; note the kink correction around 1980, which shows that the so-called law is only an approximation. [Source: Intel Corporation]

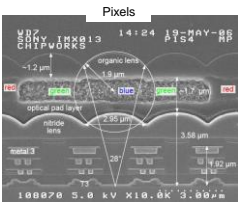
<http://www.wsj.com/articles/moores-law-runs-out-of-gas-1429282819>
 Moore's Law: More or Less? May, 2007 by Neil J. Gunther



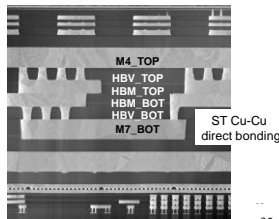
TSMC 65 nm Poly and Substrate-Chipworks



65 nm TI Baseband Chip for Nokia



Pixels

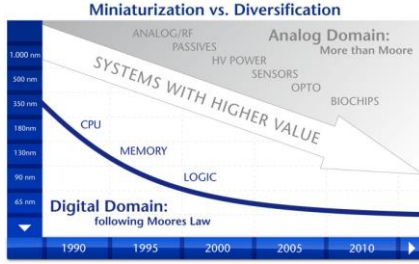


ST Cu-Cu direct bonding

"More than Moore"

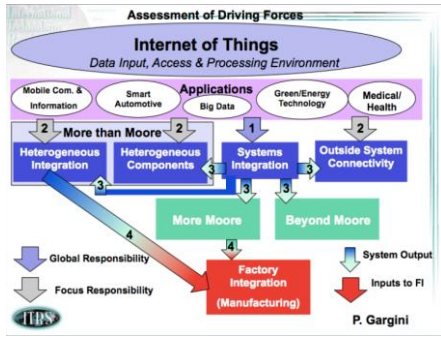
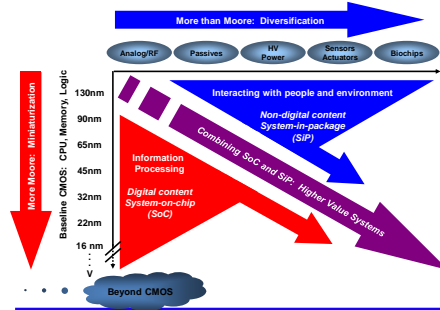
- Diversification of technologies within a chip or a package
 - Radio frequency (RF) devices
 - Power management subsystems
 - Passive components
 - Biochips
 - Sensors
 - Actuators
 - Microelectromechanical systems (MEMS)
- Integrating analog functions into CMOS-based specialty technologies enables cost-optimized and value-added system solutions.

More than Moore



Moore's Law & More

ITRS public conference San Francisco July 13, 2010

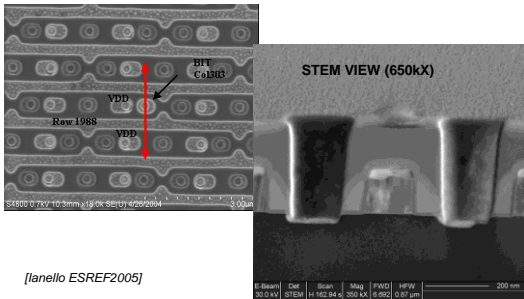


The Different Ages of Scaling (Different methods for different times)

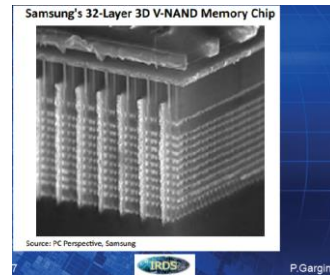
- Geometrical Scaling (1975-2003)**
 Reduction of horizontal and vertical physical dimensions in conjunction with improved performance of planar transistors
- Equivalent Scaling (2003~2021)**
 Reduction of only horizontal dimensions in conjunction with introduction of new materials and new physical effects. New vertical structures replace the planar transistor.
- 3D Power Scaling (2021~203X)**
 Transition to complete vertical device structures. Heterogeneous integration in conjunction with reduced power consumption become the technology drivers.

April 2017 | IRDS | P. Gargini

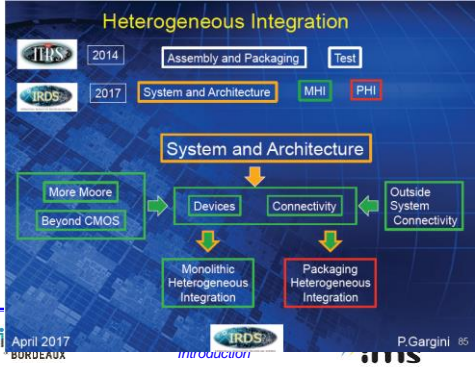
Pitch reduction



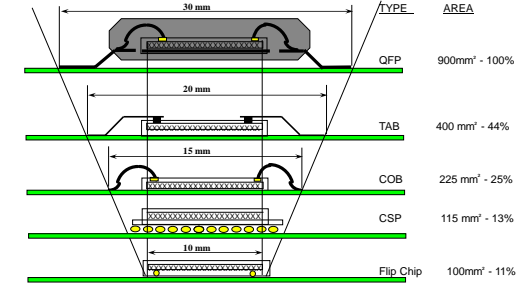
3 D integration



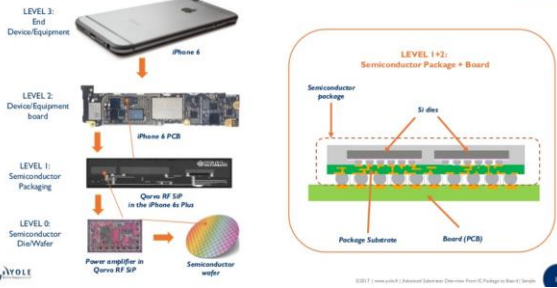
Function complexification



Report on PCB



SYSTEM INTEGRATION LEVELS

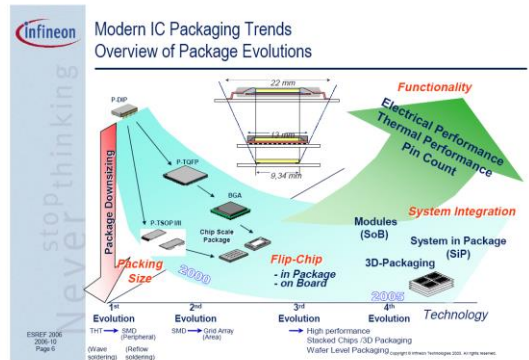
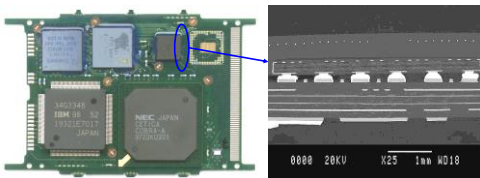


Case evolution



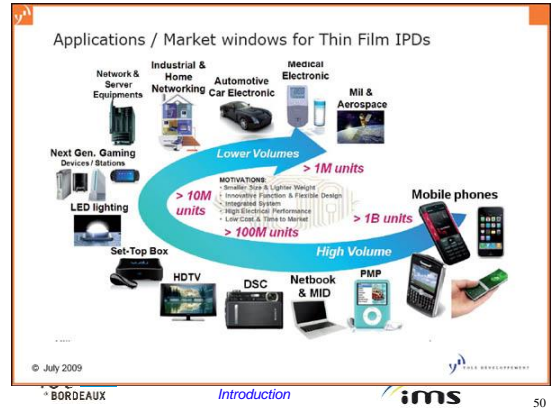
Example: complex composite assembly

- Technological parameters
 - Geometries, dimensions
 - Materials
 - Soldering/ adhesive bonding
 - Case types
 - Number of interconnection layers

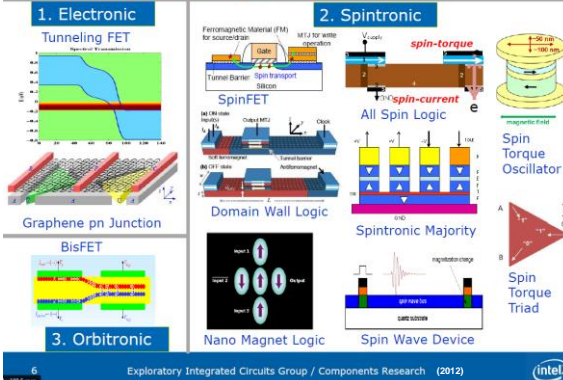


Challenges

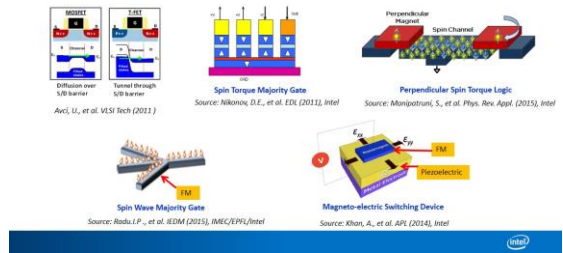
- Multi-scale in both geometric and time domains
- Multi-technology, multi-loading and multi-discipline
- Multi-material and multi-interface
- Multi-failure mechanism, multi-failure mode and multifailure location
- Strongly non-linearity
- Stochastic in nature
- Strongly time and temperature dependent



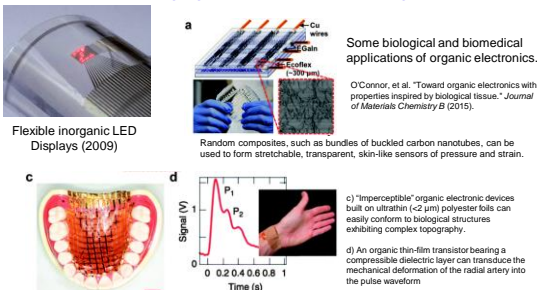
Beyond CMOS Devices



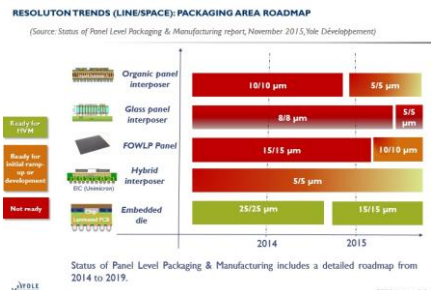
Beyond-CMOS Device Options Intel is Investigating



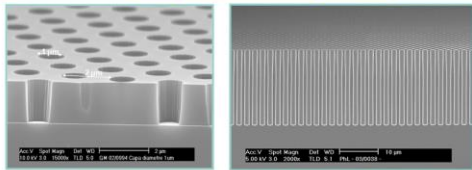
Emerging materials and technologies



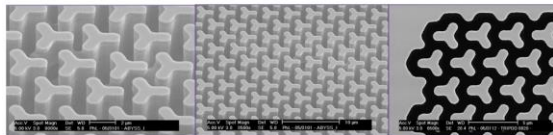
Emerging materials and technologies



NXP Two types of pit capacitors: 25 and 80 nF/mm²



PISC1: 25nF/mm², sold in more than 150M SiP devices



PISC2: 80nF/mm², Just qualified – 250nF/mm² demonstrated

Reliability: challenges

- Reliability is an important factor in any semiconductor or packaging process technology development.
- As a consequence of the strong reduction in geometries, the internal electrical fields and current densities are continuously increasing, leading to a number of reliability problems, such as
 - time-dependent dielectric breakdown,
 - hot carrier degradation,
 - electro-migration
 - stress induced voiding, etc.

Reliability

- The devices and circuits are becoming more vulnerable to effects such as electrostatic discharge (ESD), which strongly limits not only the reliability but also the yield of the circuits.
- New materials, such as high-k gate dielectrics and Cu and low-k materials, and new device architectures such as multiple gate FETs as well as new technologies like micro-electromechanical systems (MEMS) and packaging technologies are introduced.
- For these new materials, devices and technologies the failure mechanisms are still not well understood and their speed of introduction exceeds the capability to explore their reliability.

Challenges linked to new technologies

- Multi-scale in both geometric and time domains
- Multi-technology, multi-loading and multi-discipline
- Multi-material and multi-interface
- Multi-failure mechanism, multi-failure mode and multi-failure location
- Strongly non-linearity
- Stochastic in nature
- Strongly time and temperature dependent