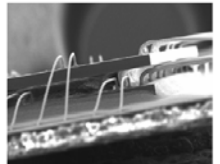
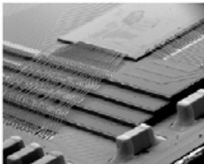
Micro and Nano- Electronics Reliability
Classical approach and new trends
PART 2_0 : Electrostatic Discharges





Triboelectricity

- The most important type of charge separation involves the contact and friction between solids known as triboelectricity. When two solid materials, A and B, contact and possibly rub against each other, electrons could move across the interface.
  - Metals

    Triboelectrification may happen when the two contacting materials are metals. When two metals contact, a voltage difference is established across the interface, with a magnitude from a couple of tenths to a few volts.

    If the metals are "well-defined" metals, the contact potential difference can be calculated from the work functions, the energy it takes to remove a loosely bound electron from the metal.
  - Insulators

    It is conceivable that only electrons located close to the surface can participate in the charging of highly isolative materials. Similar to metals, for some of these materials it is possible to measure the work function for loosely bound electrons.

Electro-Static Discharges

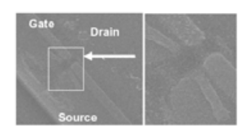


Figure 9. SEM micrograph of a device without ESD implant showing the failure signature (drain to source short)

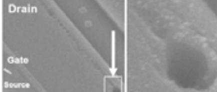


Figure 10. SEM micrograph of a device with ESD implant showing the failure signature (damage on drain contacts).

D. Alvareza, et Al *Analysis of ESD failure mechanism in 65nm bulk CMOS ESD* (ESREF 2006)

TRIBOELECTRIC SERIES

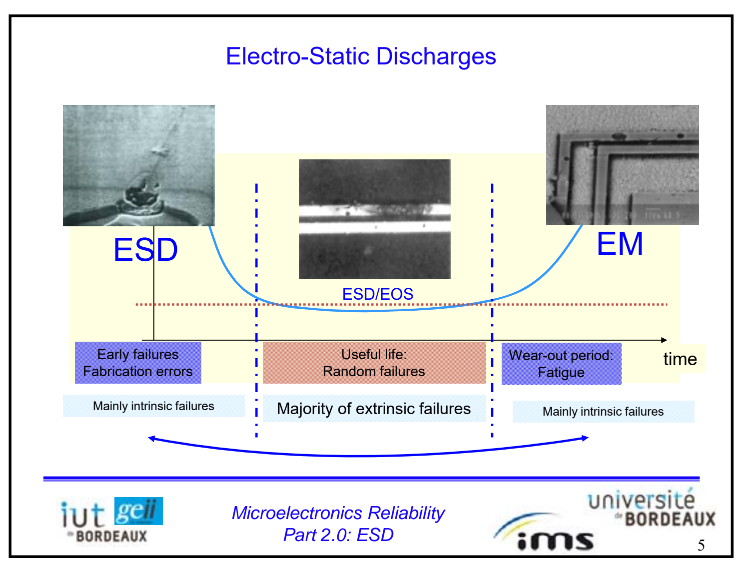
MATERIALS	POLARITY	
Acetate	+	—
Glass	+	—
Human Hair	+	—
Nylon	+	—
Lead	+	—
Aluminum	+	—
Paper	+	—
Polyurethane	+	—
Cotton	+	—
Steel	+	—
Hard Rubber	+	—
Acetate Fiber	+	—
MYLAR*	+	—
Epoxy Glass	+	—
Nickel, Copper, Silver	+	—
UV Resist	+	—
Stainless Steel	+	—
Synthetic Rubber	+	—
Acrylic	+	—
Polystyrene Foam	+	—
Polyurethane Foam	+	—
Polyester	+	—
Polyethylene	+	—
Polypropylene	+	—
PVC (Vinyl)	+	—
TEFLON*	+	—
Silicone Rubber	+	—

* Trademark of E.I. Du Pont

Figure 2 Triboelectric Series Chart

Triboelectricity

- The relative positioning of the materials governs the magnitude and polarity of the charge that results when the materials contact and separate.
- The farther apart the materials are in the series, the greater the magnitude of the charge.


Electro-Static Discharges
ESD
EM
ESD/EOS
Early failures
Fabrication errors
Useful life:
Random failures
Wear-out period:
Fatigue
time
Mainly intrinsic failures
Majority of extrinsic failures
Mainly intrinsic failures
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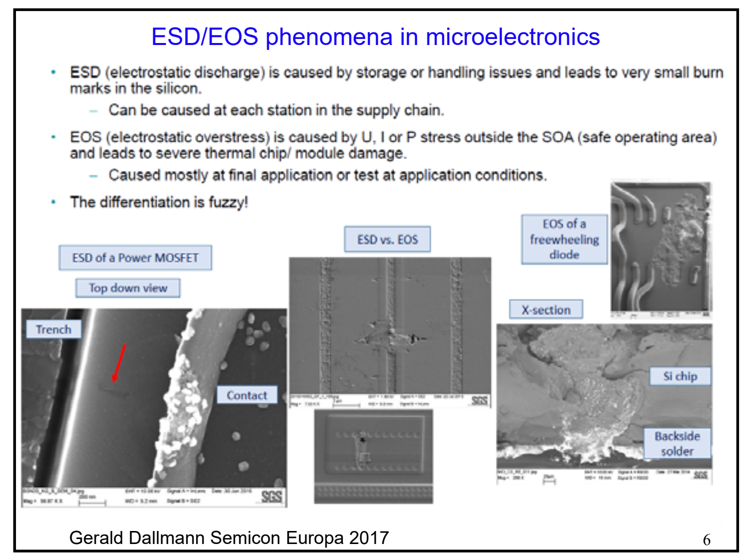
ESD/EOS phenomena in microelectronics
• ESD (electrostatic discharge) is caused by storage or handling issues and leads to very small burn marks in the silicon.
– Can be caused at each station in the supply chain.
• EOS (electrostatic overstress) is caused by U, I or P stress outside the SOA (safe operating area) and leads to severe thermal chip/ module damage.
– Caused mostly at final application or test at application conditions.
• The differentiation is fuzzy!
ESD of a Power MOSFET
Top down view
Trench
Contact
ESD vs. EOS
EOS of a freewheeling diode
X-section
Si chip
Backside solder
Gerald Dallmann Semicon Europa 2017
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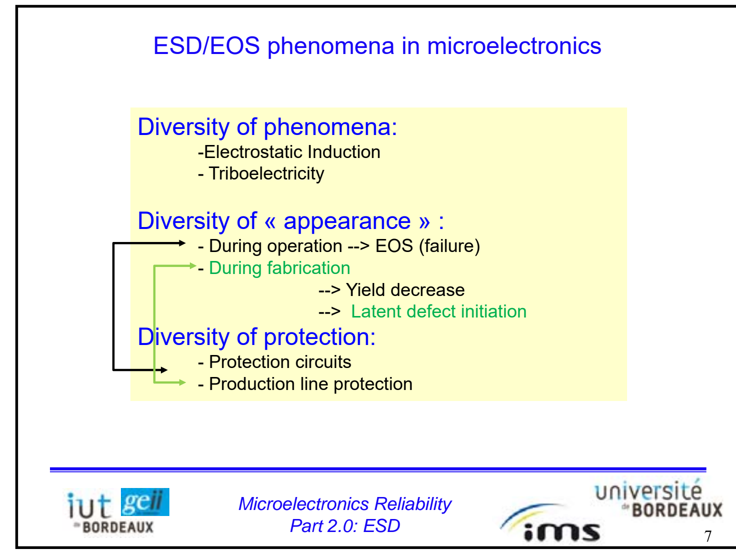
ESD/EOS phenomena in microelectronics
Diversity of phenomena:
-Electrostatic Induction
- Triboelectricity
Diversity of « appearance » :
- During operation --> EOS (failure)
- During fabrication
--> Yield decrease
--> Latent defect initiation
Diversity of protection:
- Protection circuits
- Production line protection
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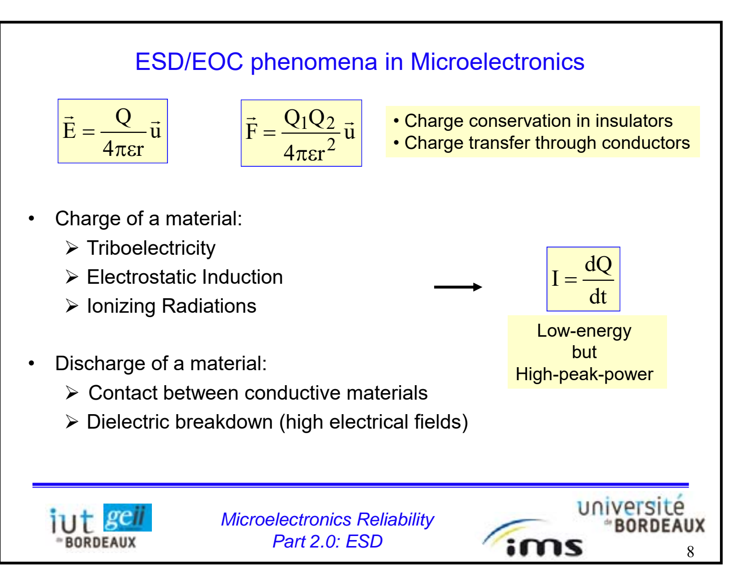
ESD/EOC phenomena in Microelectronics
$\vec{E} = \frac{Q}{4\pi\varepsilon r}\vec{u}$
$\vec{F} = \frac{Q_1 Q_2}{4\pi\varepsilon r^2}\vec{u}$
• Charge conservation in insulators
• Charge transfer through conductors
• Charge of a material:
➢ Triboelectricity
➢ Electrostatic Induction
➢ Ionizing Radiations
$I = \frac{dQ}{dt}$
Low-energy
but
High-peak-power
• Discharge of a material:
➢ Contact between conductive materials
➢ Dielectric breakdown (high electrical fields)
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Electrostatic induction

- In operational conditions, electrostatic induction through :
  - Video monitor
  - High voltage DC supplies
  - Natural phenomena (Storm)
  - Latex
  - Teflon
  - Plastic packages
  - ….

charged (Latex, Teflon, Plastic packages)

Electrostatic potential

	10%	40%	55% RH
Person walking on a carpet	35	15	7.5
Person walking on a vinyl floor	12	5	3
Operator on a bench	6	0.5	0.4
Ceramic cases in a plastic container	2	0.7	0.4
Ceramic cases in a vinyl container	11.5	4	2
Ceramic cases in polystyrene	14.5	5	3.5
Circuits when opening bag	25	20	7
Circuits in automatic pick and place	21	11	5.5

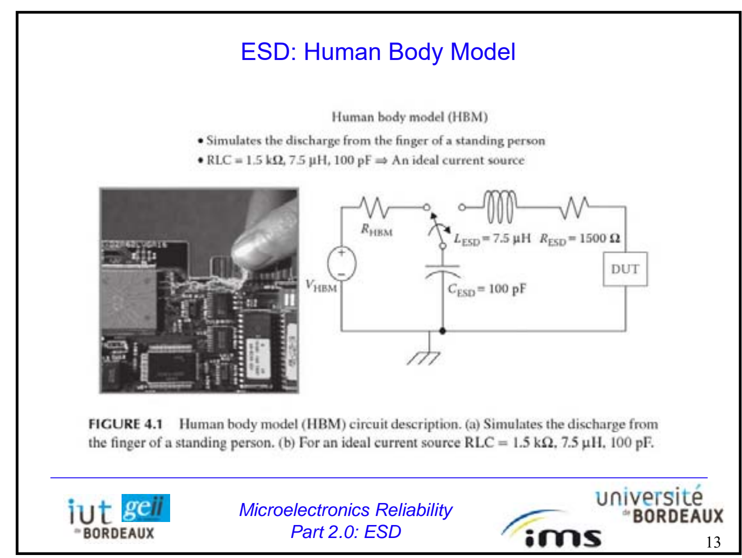
(kV)

ESD sensitivity of different technologies (in V)

	Usual techno	Optimized techno
MOSFET	100	200
JFET	140	10000
CMOS	250	2000
Schottky diodes, TTL	300	2500
Bipolar transistors	300	7000
ECL	500	-

Industry-standard ESD models

- Electrostatic discharge (ESD) occurs in a variety of ways, depending on where and how the static charge is accumulated and how the charge build-up is dissipated.
- There are 3 industry-standard ESD models that define how semiconductor devices are to be tested for ESD sensitivity under different situations of electrostatic build-up and discharge:
  - Human Body Model (HBM)
  - Machine Model (MM).
  - Charged Device Model (CDM)


ESD: Human Body Model
Human body model (HBM)
• Simulates the discharge from the finger of a standing person
• RLC = 1.5 kΩ, 7.5 µH, 100 pF ⇒ An ideal current source
R_{HBM}
L_{ESD} = 7.5 µH
R_{ESD} = 1500 Ω
DUT
V_{HBM}
C_{ESD} = 100 pF
FIGURE 4.1 Human body model (HBM) circuit description. (a) Simulates the discharge from the finger of a standing person. (b) For an ideal current source RLC = 1.5 kΩ, 7.5 µH, 100 pF.
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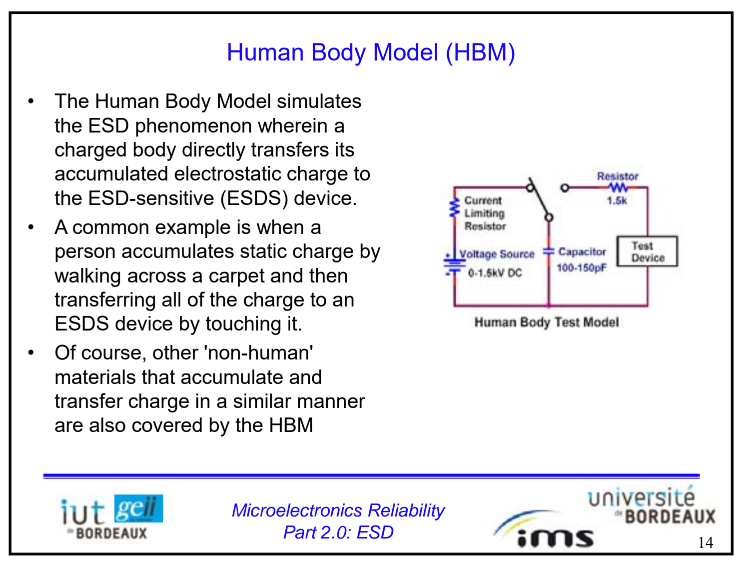
Human Body Model (HBM)
• The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive (ESDS) device.
• A common example is when a person accumulates static charge by walking across a carpet and then transferring all of the charge to an ESDS device by touching it.
• Of course, other 'non-human' materials that accumulate and transfer charge in a similar manner are also covered by the HBM
Current Limiting Resistor
Resistor
1.5k
Voltage Source
0-1.5kV DC
Capacitor
100-150pF
Test Device
Human Body Test Model
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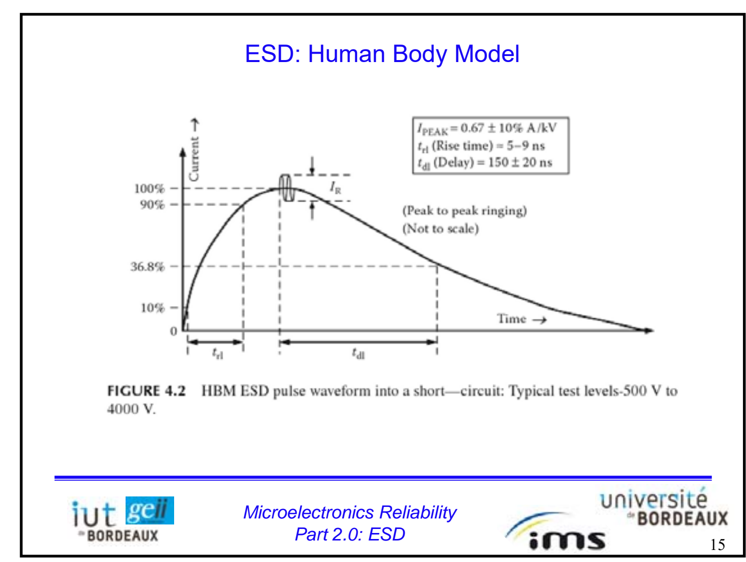
ESD: Human Body Model
I_{PEAK} = 0.67 ± 10% A/kV
t_{ri} (Rise time) = 5–9 ns
t_{dl} (Delay) = 150 ± 20 ns
Current
100%
90%
36.8%
10%
0
I_R
(Peak to peak ringing)
(Not to scale)
Time →
t_{ri}
t_{dl}
FIGURE 4.2 HBM ESD pulse waveform into a short—circuit: Typical test levels-500 V to 4000 V.
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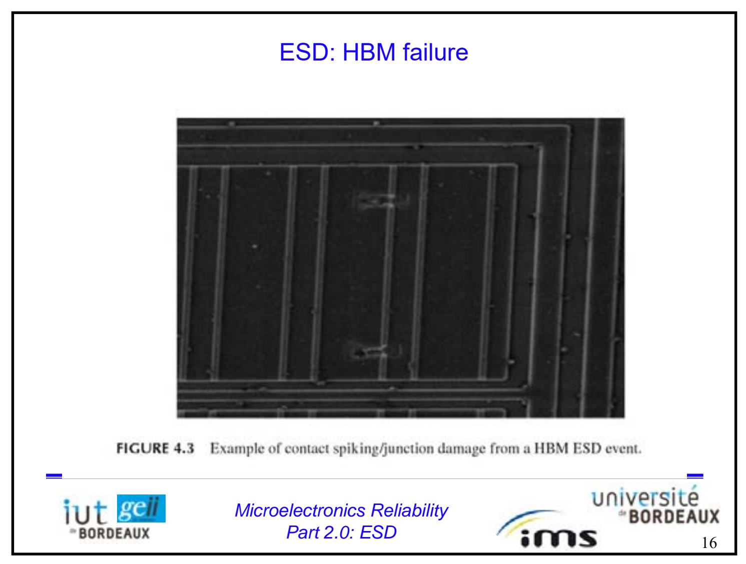
ESD: HBM failure
FIGURE 4.3 Example of contact spiking/junction damage from a HBM ESD event.
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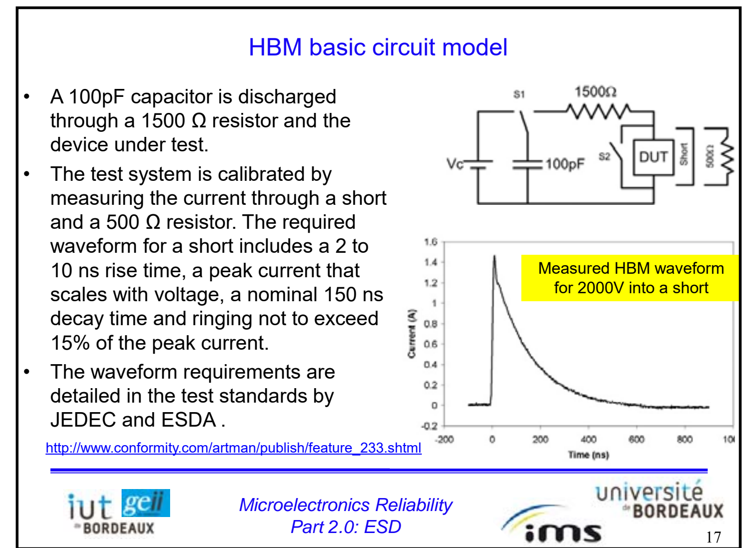
HBM basic circuit model
• A 100pF capacitor is discharged through a 1500 Ω resistor and the device under test.
• The test system is calibrated by measuring the current through a short and a 500 Ω resistor. The required waveform for a short includes a 2 to 10 ns rise time, a peak current that scales with voltage, a nominal 150 ns decay time and ringing not to exceed 15% of the peak current.
• The waveform requirements are detailed in the test standards by JEDEC and ESDA .
http://www.conformity.com/artman/publish/feature_233.shtml
S1
1500Ω
Vc
100pF
S2
DUT
Short
500Ω
Measured HBM waveform for 2000V into a short
Current (A)
Time (ns)
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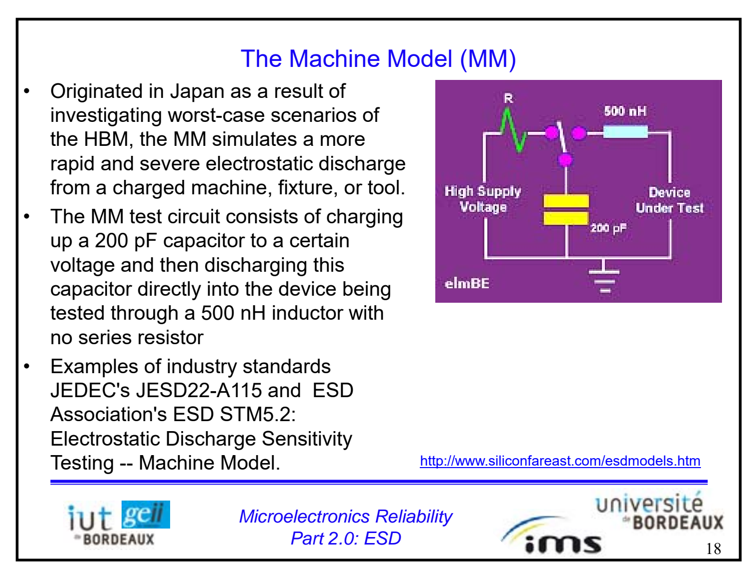
The Machine Model (MM)
• Originated in Japan as a result of investigating worst-case scenarios of the HBM, the MM simulates a more rapid and severe electrostatic discharge from a charged machine, fixture, or tool.
• The MM test circuit consists of charging up a 200 pF capacitor to a certain voltage and then discharging this capacitor directly into the device being tested through a 500 nH inductor with no series resistor
• Examples of industry standards JEDEC's JESD22-A115 and ESD Association's ESD STM5.2: Electrostatic Discharge Sensitivity Testing -- Machine Model.
R
500 nH
High Supply Voltage
Device Under Test
200 pF
eImBE
http://www.siliconfareast.com/esdmodels.htm
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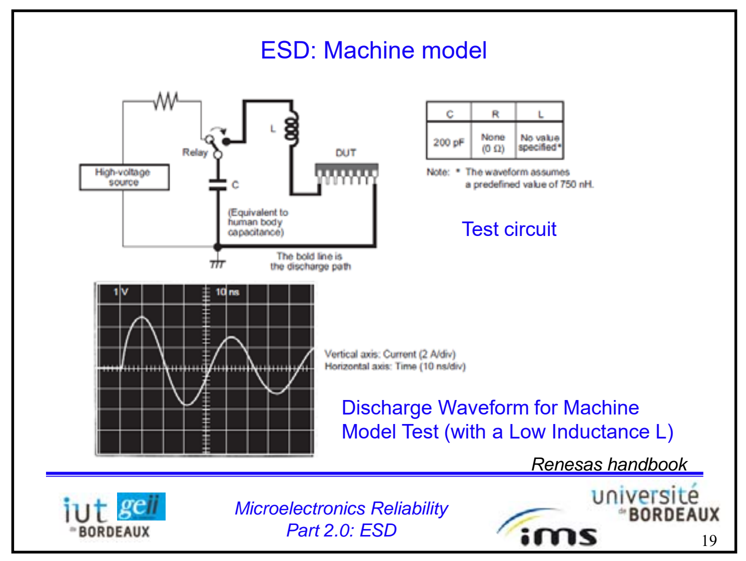
ESD: Machine model
High-voltage source
Relay
L
C
DUT
(Equivalent to human body capacitance)
The bold line is the discharge path
C | R | L
200 pF | None (0 Ω) | No value specified*
Note: * The waveform assumes a predefined value of 750 nH.
Test circuit
1 V
10 ns
Vertical axis: Current (2 A/div)
Horizontal axis: Time (10 ns/div)
Discharge Waveform for Machine Model Test (with a Low Inductance L)
Renesas handbook
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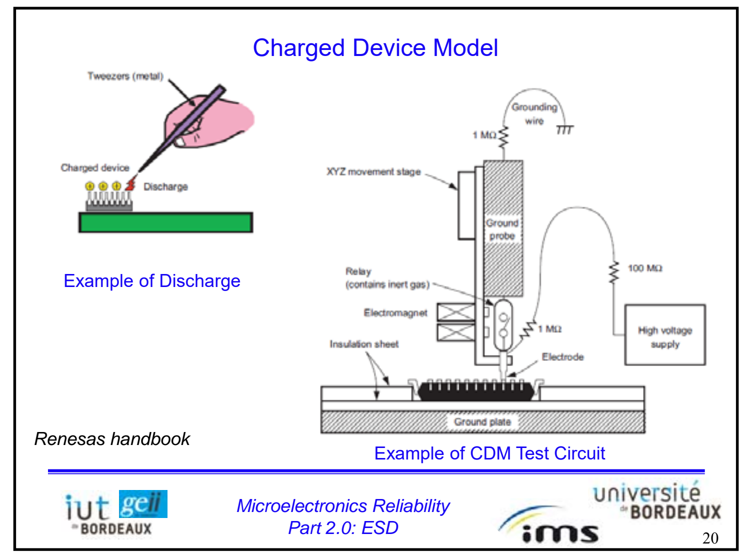
Charged Device Model
Tweezers (metal)
Charged device
Discharge
Example of Discharge
Grounding wire
1 MΩ
XYZ movement stage
Ground probe
100 MΩ
Relay (contains inert gas)
Electromagnet
1 MΩ
High voltage supply
Insulation sheet
Electrode
Ground plate
Renesas handbook
Example of CDM Test Circuit
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Charged Device Model (CDM)

- Not all ESD events involve the transfer of charge into the device. Electrostatic discharge from a charged device to another body is also a form of ESD, and a quite commonly encountered one at that.
- A device can accumulate charge in a variety of ways, especially in situations where they undergo movement while in contact with another object, such as when sliding down a track or feeder. If they come into contact with another conductive body that is at a lower potential, it discharges into that body. Such an ESD event is known as Charged Device Model ESD, which can even be more destructive than HBM ESD (despite its shorter pulse duration) because of its high current.
- Discharge Sensitivity Testing -- Charged Device Model.

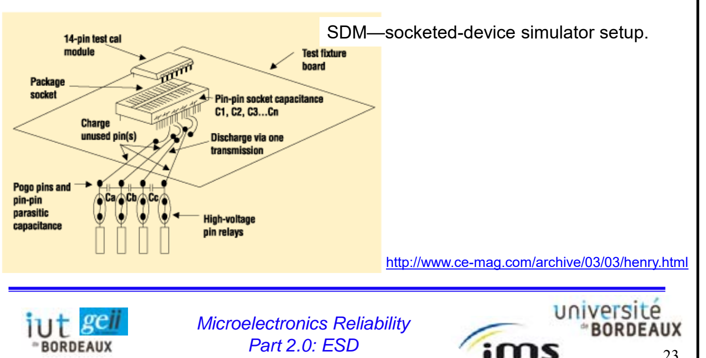
Charged Device Model (CDM) testing

- Socketted Discharge Model (SDM)
  - SDM simulates a device inserted in a socket, then charged from a high voltage source, and then discharged through a 1Ω resistor.
  - SDM is easy to conduct but is not always replicating real-world CDM ESD events.

Fig. 5. A typical CDM ESD discharging waveform at a discharge level of ~1100 V[11].

Real-world Charged Device Model (RCDM).

- RCDM testing consists of putting the DUT in deadbug position on a thin dielectric (FR4), which is then placed over a ground plate. The DUT is then charged either directly by a charging probe or indirectly by field induction. Each pin is then discharged through a 1-ohm resistor to ground.



SDM—socketed-device simulator setup.

http://www.ce-mag.com/archive/03/03/henry.html

ESD Failures

- Direct ESD to devices may cause failures either through voltage breakdown damage to insulating oxide layers, or energy related damage to junction, metallisation and other features.
- Oxide dielectric breakdown
  - Oxide layers are commonly used to insulate the gate in MOSFETs and metallisation in other devices. If the breakdown field strength of this oxide layer is exceeded, dielectric breakdown can occur. A subsequent current flow in a discharge through the gate rupture can melt silicon and form a conducting bridge.
  - Where subsequent current flow does not have sufficient energy to cause a short circuit, the device may continue to operate. It may have a detectable increased leakage current. The device may be weakened and prone to failure later. This is known as latent damage, and damaged devices are often referred to as the 'walking wounded'.

ESD Failures

- Junction burnout
  - An ESD event may pass through a transistor junction. The high current causes local heating, especially if the short timescale does not allow heat flow to the surrounding regions. Higher temperature material has a reduced resistance and attracts further current flow – a hot spot can form that may lead to melting and short-circuit of the junction.
  - Migration of a metal ‘spike’ across a diffusion layer can also occur as a result of thermal damage.

ESD Failures

- Metallisation melt
  - Metallisation melt or burnout happens when the current in an interconnection track is high enough to raise the temperature to melting point. The metallisation burns out like a fuse, and an open circuit track results.

- Latch-up
  - Latch-up is a problem in powered CMOS devices caused by the inadvertent turn-on and latching of parasitic SCR structures in the device structure. Large currents can flow, leading to thermal damage. Latch-up can be a result of an ESD event or transient on power, input and output lines.

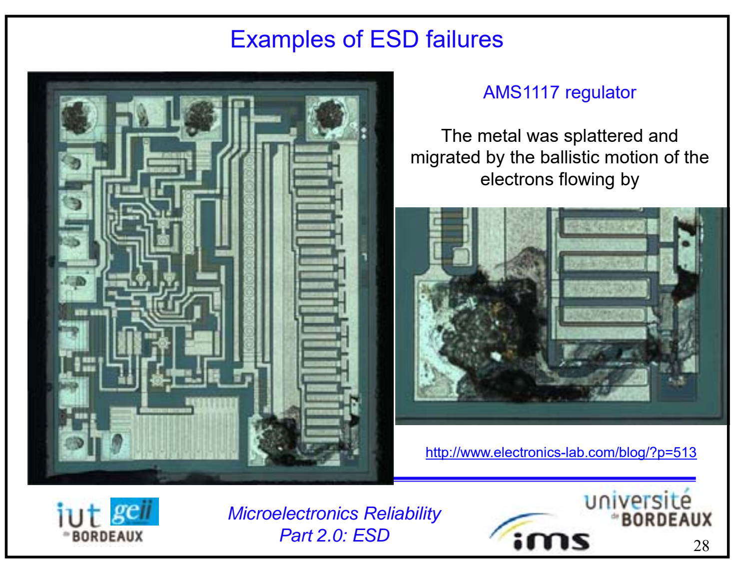
http://www.ami.ac.uk/courses/topics/0181_ftes/

ESD : Rogue failures

- ESD may induce latent failure:
  - no effect at t=0
  - distribution of failures appear during the life
  - very difficult to identify during the failure analysis

    - to be compared to an informatics virus

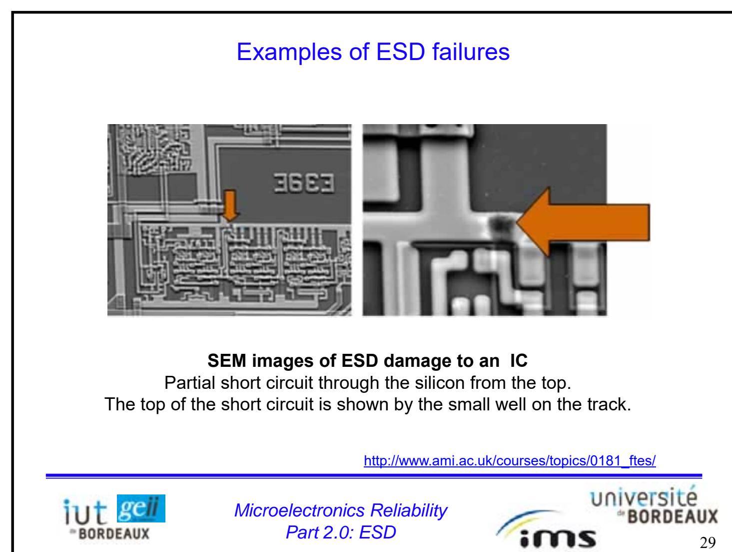
Examples of ESD failures



AMS1117 regulator

The metal was splattered and migrated by the ballistic motion of the electrons flowing by

http://www.electronics-lab.com/blog/?p=513


Examples of ESD failures
SEM images of ESD damage to an IC
Partial short circuit through the silicon from the top.
The top of the short circuit is shown by the small well on the track.
http://www.ami.ac.uk/courses/topics/0181_fes/
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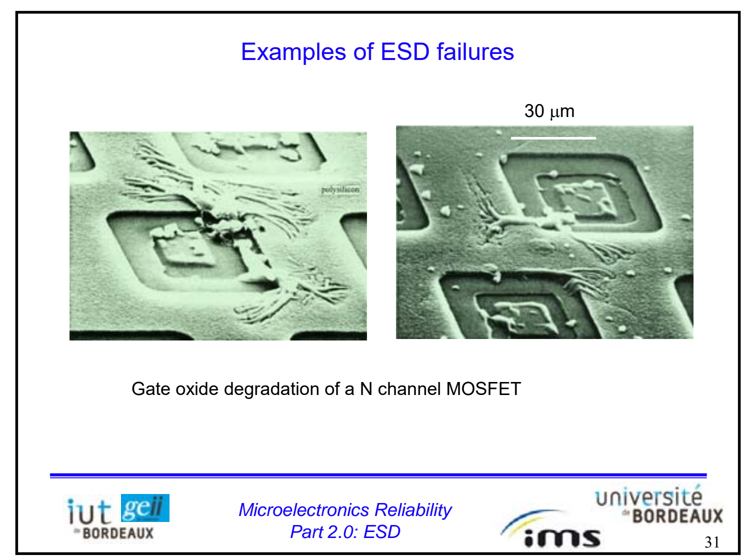
Examples of ESD failures
30 µm
Gate oxide degradation of a N channel MOSFET
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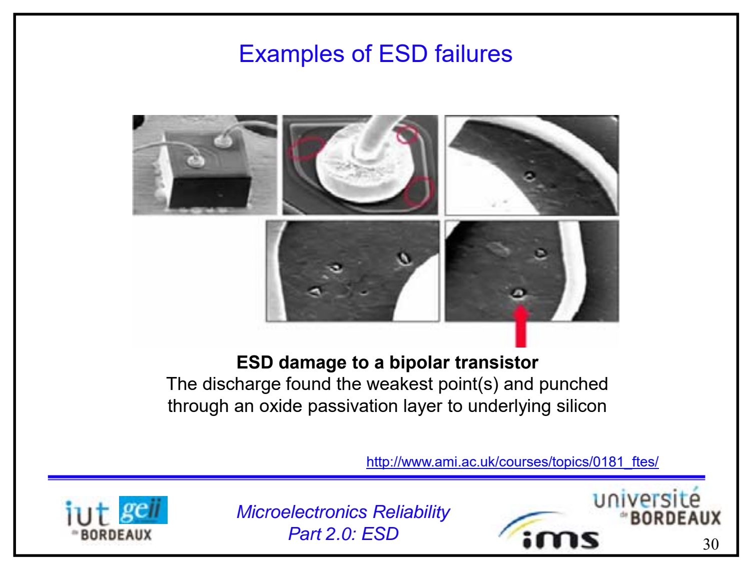
Examples of ESD failures
ESD damage to a bipolar transistor
The discharge found the weakest point(s) and punched through an oxide passivation layer to underlying silicon
http://www.ami.ac.uk/courses/topics/0181_fes/
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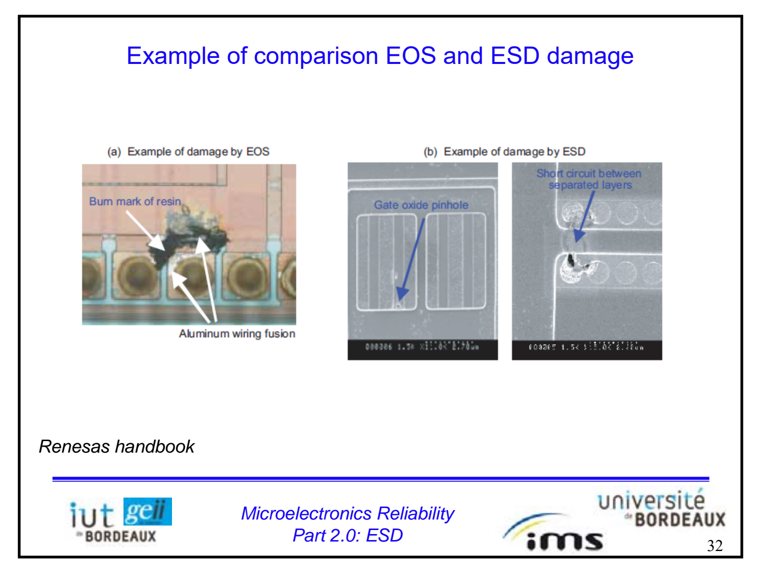
Example of comparison EOS and ESD damage
(a) Example of damage by EOS
Burn mark of resin
Aluminum wiring fusion
(b) Example of damage by ESD
Gate oxide pinhole
Short circuit between separated layers
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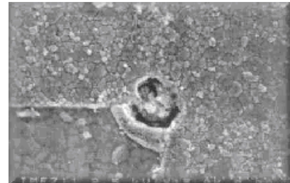
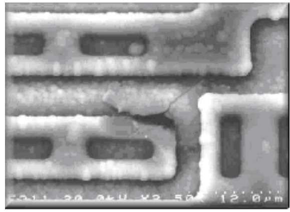
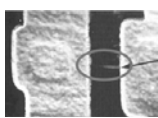
Examples of ESD failures



HBM ESD induced failure in an nMOS pad



CDM ESD induced failure in a high CMOS device core



Latent ESD failure

ESD: Protection in the production site

SUSCEPTIBILITY

Good ESD Practices

The following guidelines will help in preventing ESD damage:

- ➢ Use good grounding practices.
- ➢ Be especially careful when wearing synthetic clothing while working with circuit boards. Clothing made of synthetics (polymers) will generate static charges while clothing made of cotton will not.
- ➢ Store parts in anti-static bags.
- ➢ Never place unprotected boards in plastic containers.
- ➢ Always touch the metal chassis before handling parts.
- ➢ Handle boards by the edges.

• Prevention is the best defense.

PROTECTION

http://www.rtitech.com/downloads/News/What%20is%20ESD.pdf

ESD: Protection in the production site

- In places where components and circuit-boards are handled unprotected, there should be an ESD protected area (called EPA) to avoid electro-static discharging.
- Outside the EPA all components and boards should be handled in shielded packaging.
- In order to maintain a high quality of the ESD protection, the processes for ESD safe handling should continuously be evaluated.

Wrist band, for connecting to ground

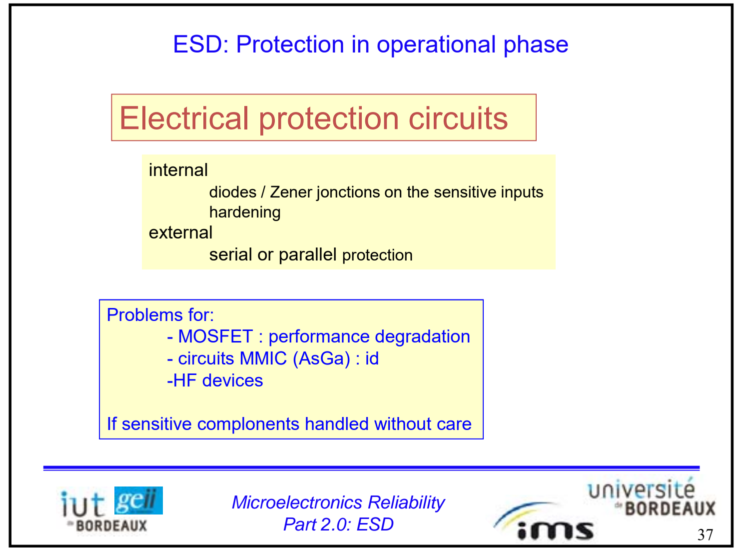
Elements for building the floor mat

ESD: Protection in the production site

ESD shoes.

ionizing fans
compressed air guns

Packing material - bags


ESD: Protection in operational phase
Electrical protection circuits
internal
diodes / Zener jonctions on the sensitive inputs
hardening
external
serial or parallel protection
Problems for:
- MOSFET : performance degradation
- circuits MMIC (AsGa) : id
-HF devices
If sensitive complonents handled without care
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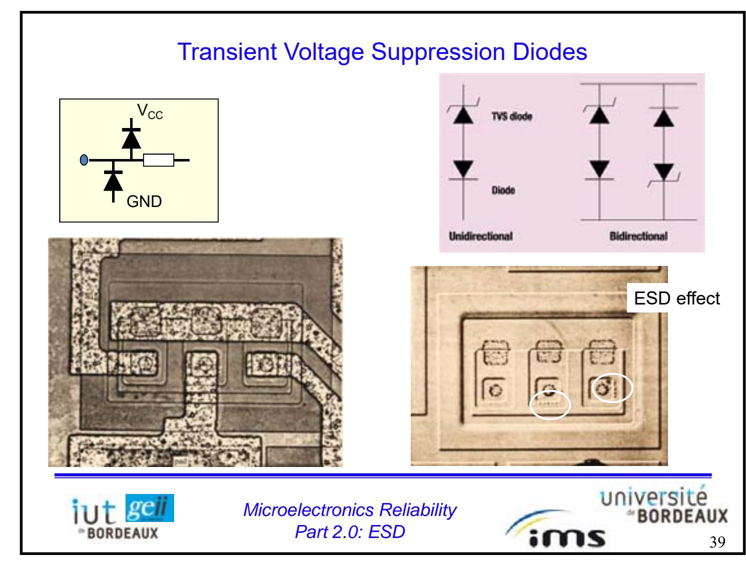
Transient Voltage Suppression Diodes
VCC
GND
TVS diode
Diode
Unidirectional
Bidirectional
ESD effect
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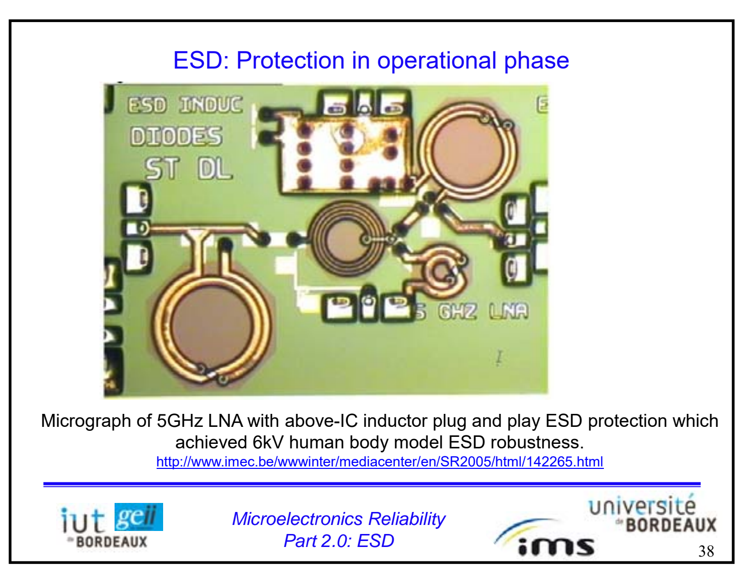
ESD: Protection in operational phase
ESD INDUC
DIODES
ST DL
5 GHZ LNA
Micrograph of 5GHz LNA with above-IC inductor plug and play ESD protection which achieved 6kV human body model ESD robustness.
http://www.imec.be/wwwinter/mediacenter/en/SR2005/html/142265.html
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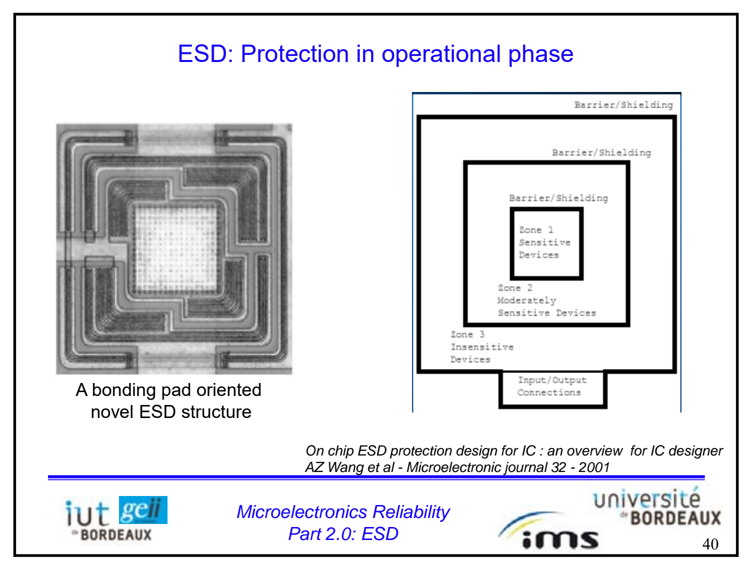
ESD: Protection in operational phase
Barrier/Shielding
Barrier/Shielding
Barrier/Shielding
Zone 1 Sensitive Devices
Zone 2 Moderately Sensitive Devices
Zone 3 Insensitive Devices
Input/Output Connections
A bonding pad oriented novel ESD structure
On chip ESD protection design for IC : an overview for IC designer
AZ Wang et al - Microelectronic journal 32 - 2001
Microelectronics Reliability
Part 2.0: ESD
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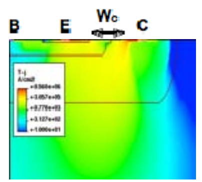
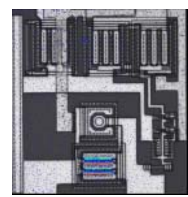
ESD: Protection in operational phase
Device modeling



Simulation of the density current distribution during the transition from ESD in a component of protection (LAAS)



Localization with microscopy light emission of an ESD failure on an integrated circuit

Bibliographic references

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3. ESD testing of devices, ICs and systems *T. Smedes* - Microelectronics Reliability, In Press, Corrected Proof, Available online 28 July 2009
4. Renesas handbook Jan. 30, 2017